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U.S. PATENT DOCUMENTS

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* cited by examiner

(57) **ABSTRACT**

An organic light emitting display device according to the present disclosure includes: a semiconductor on a substrate including a switching channel of a switching transistor and a driving channel of a driving transistor, the driving transistor being spaced from the switching transistor; a first insulating layer covering the semiconductor; a switching gate electrode on the first insulating layer and overlapping the switching channel and a driving gate electrode on the first gate insulating layer and overlapping the driving channel; a second insulating layer covering the switching gate electrode and the driving gate electrode; a data line on the second insulating layer comprising: an upper data line; and a lower data line; a driving voltage line on the second insulating layer; a passivation layer covering the data line and the driving voltage line; a pixel electrode on the passivation layer; and a first pixel connecting member on the passivation layer.

19 Claims, 15 Drawing Sheets

Sep. 15, 2014 (KR) 10-2014-0122273

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CPC ***H01L 27/3276*** (2013.01); ***H01L 27/3244***
(2013.01); ***H01L 27/3262*** (2013.01); ***H01L***
27/3265 (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/3276; H01L 27/3244
See application file for complete search history.

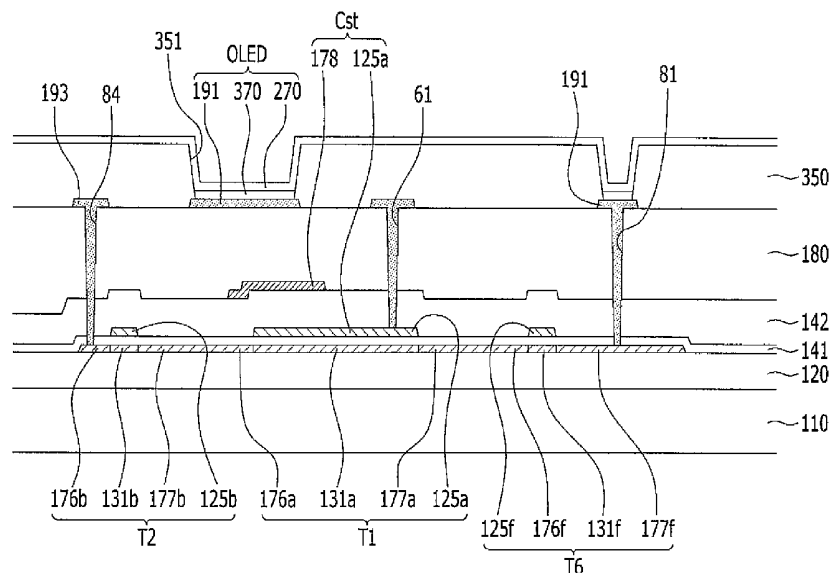


FIG. 1

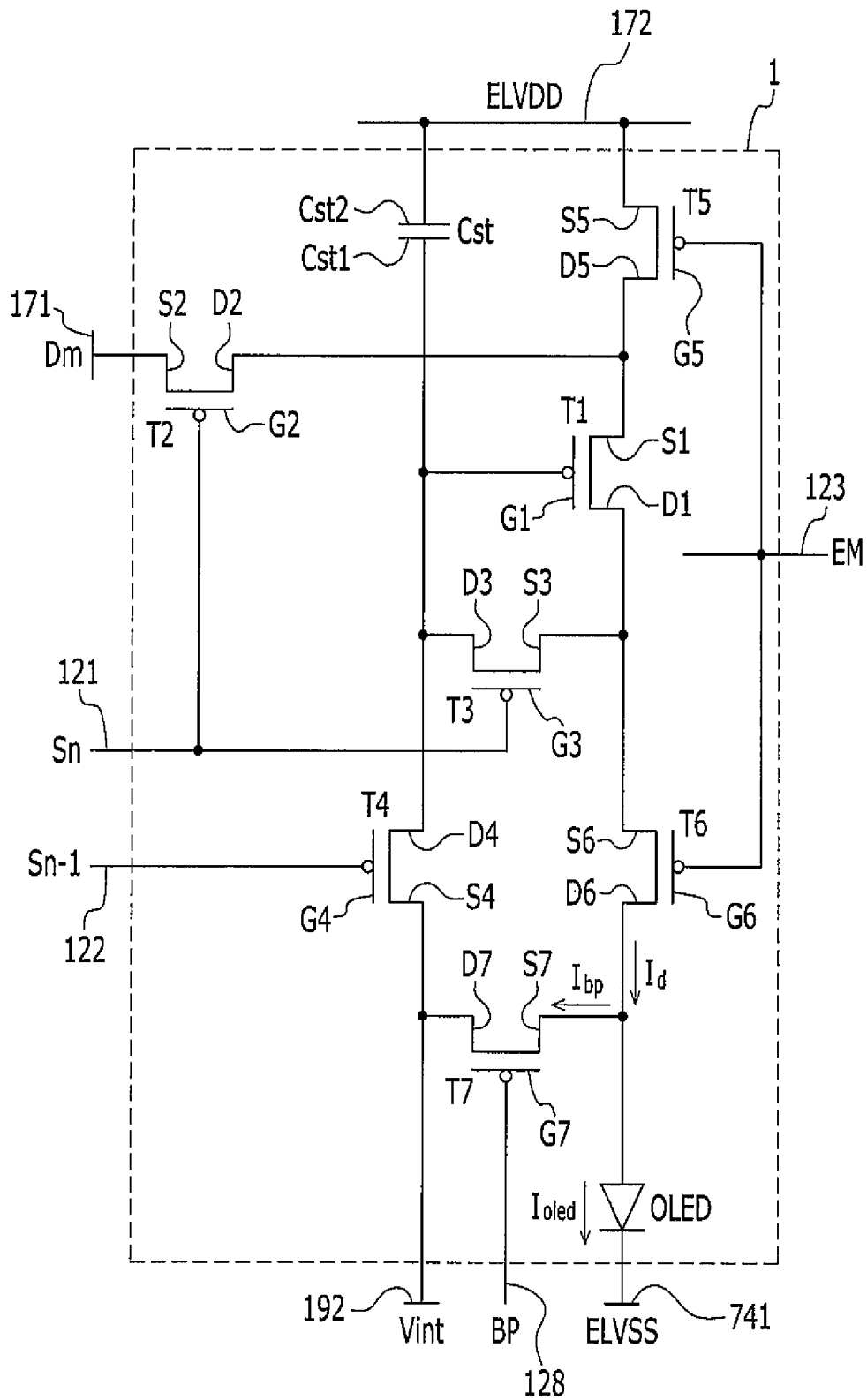


FIG. 2

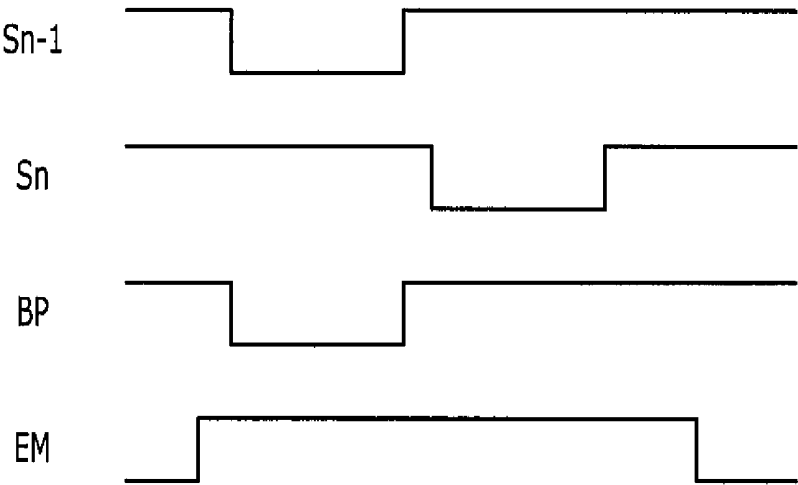


FIG. 3

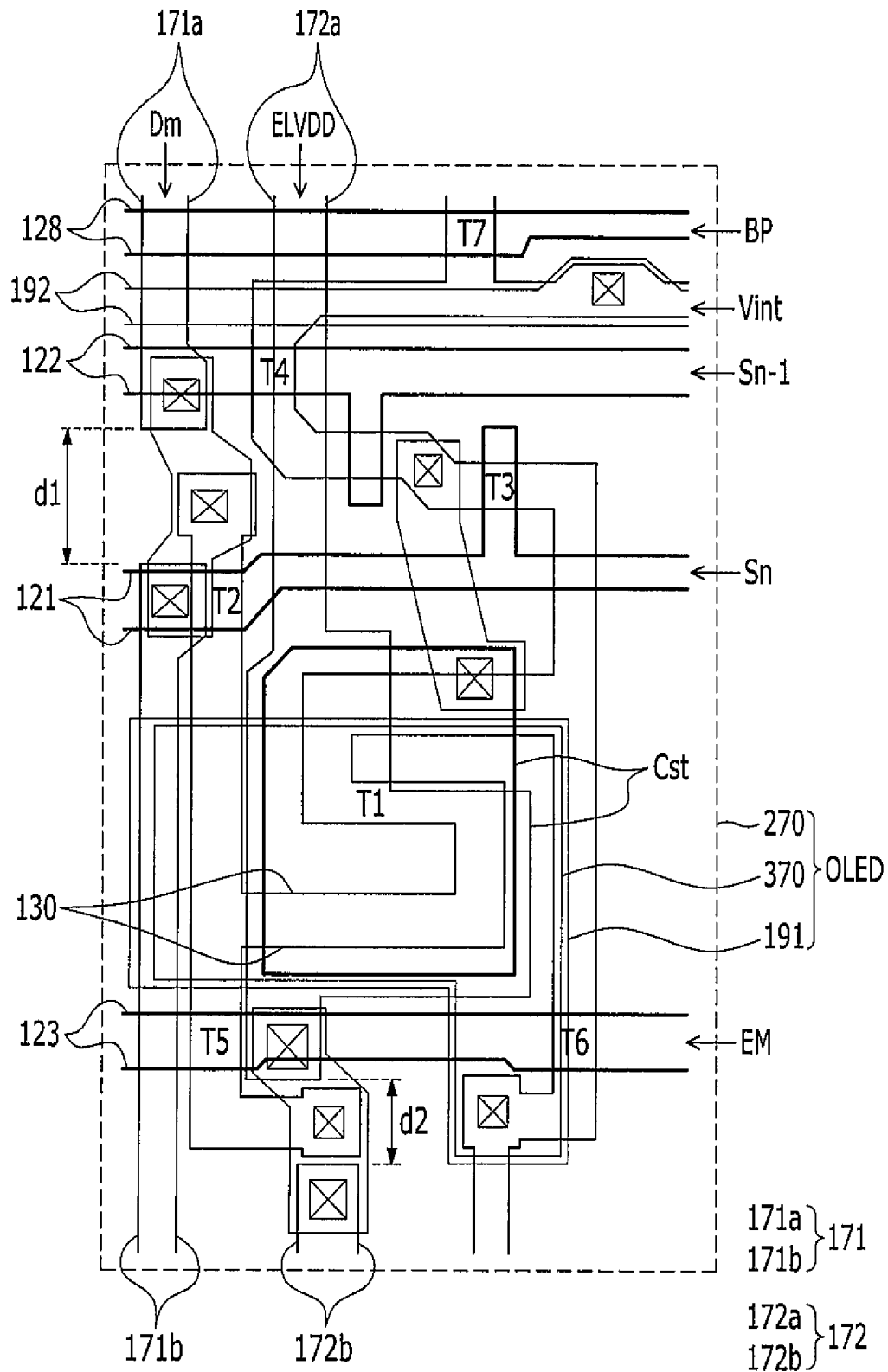


FIG. 4

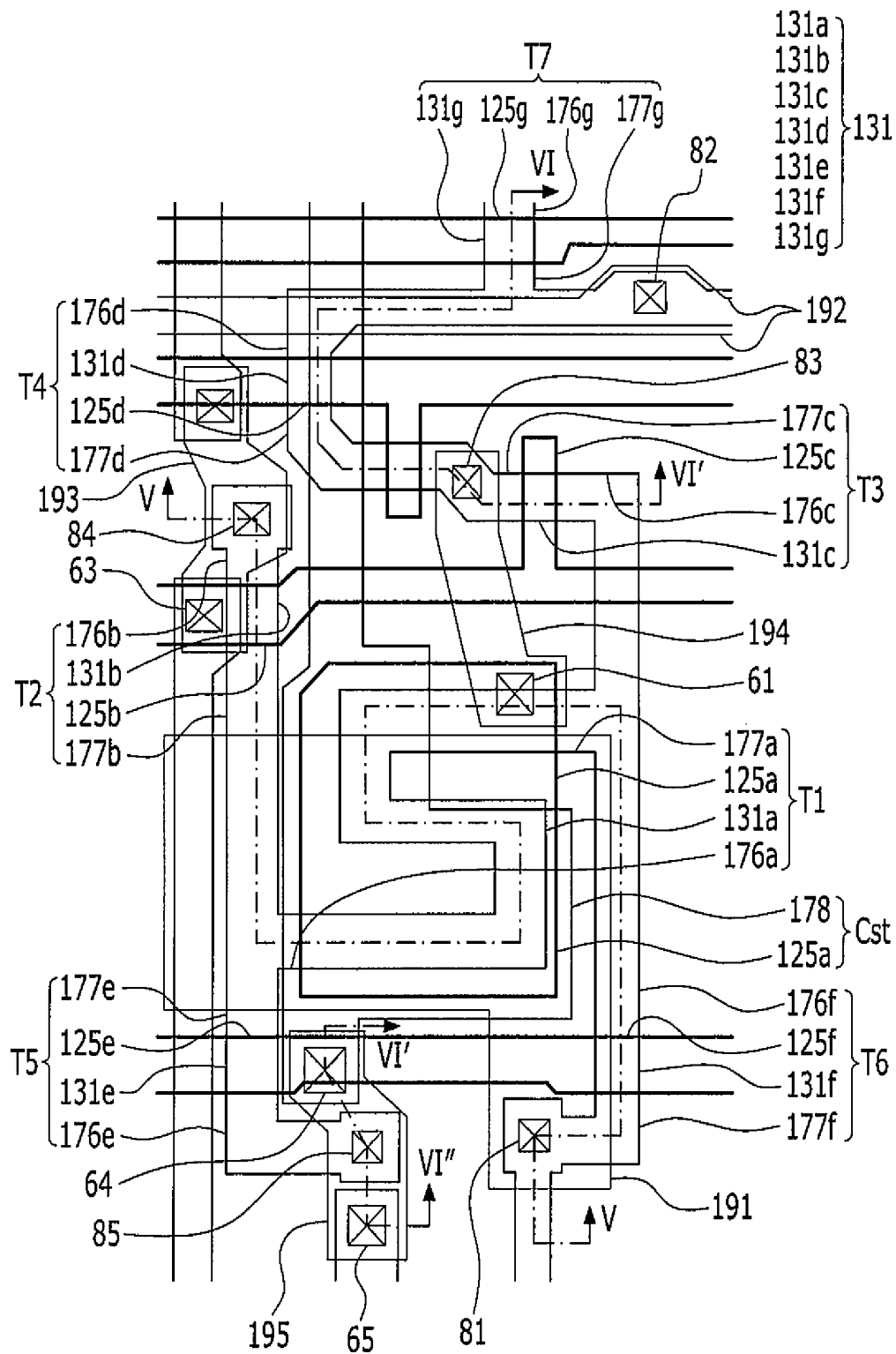


FIG. 5

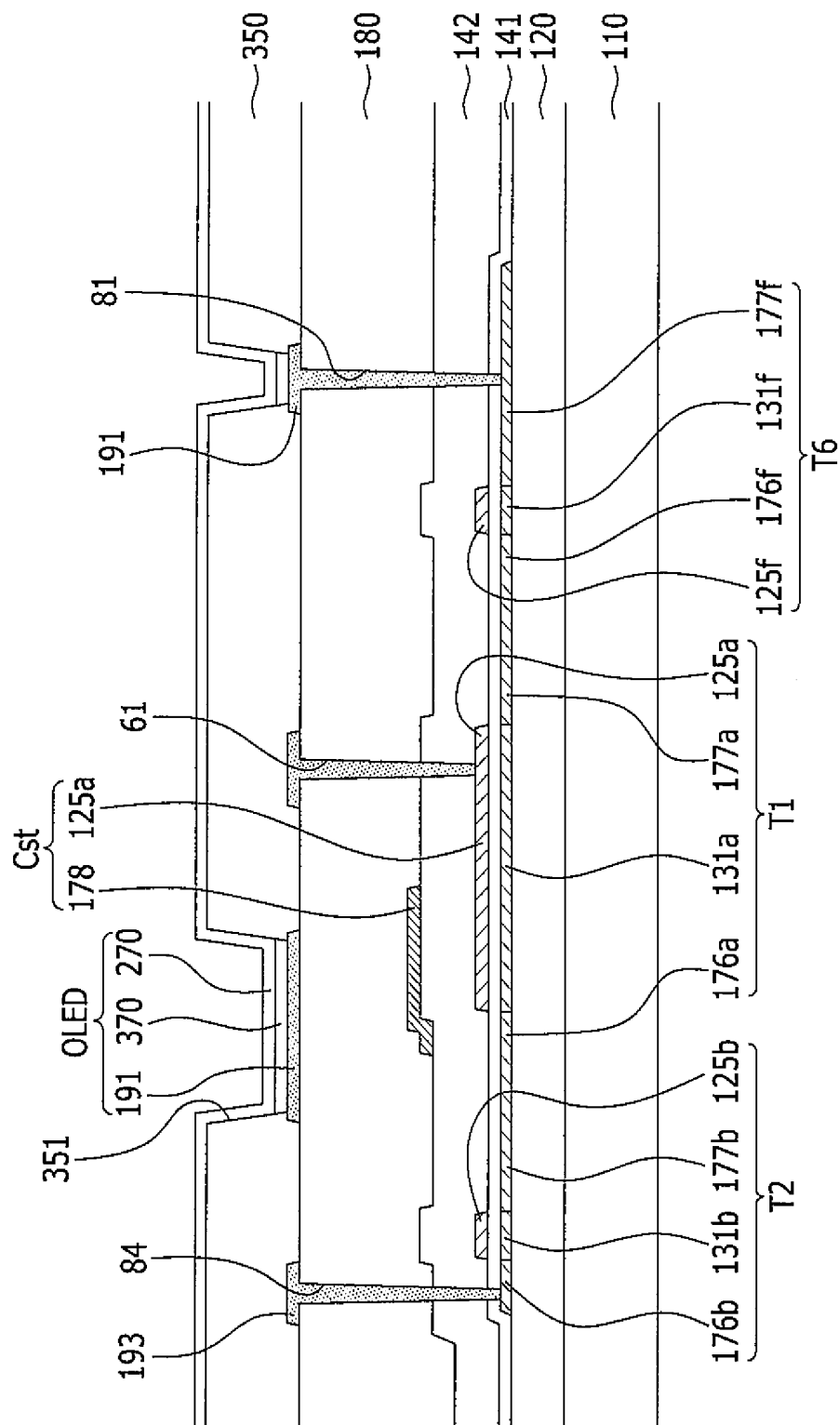


FIG. 6

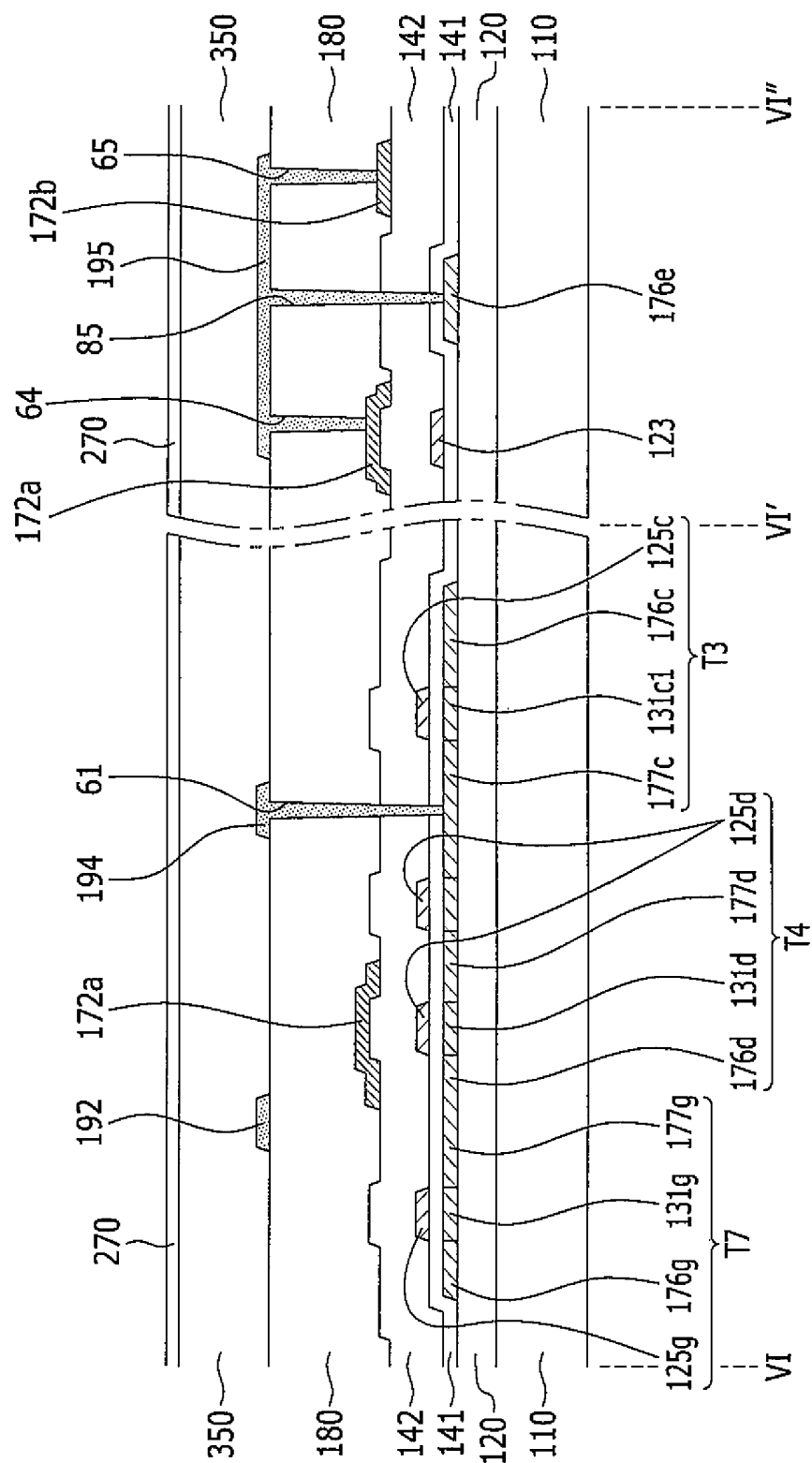


FIG. 7

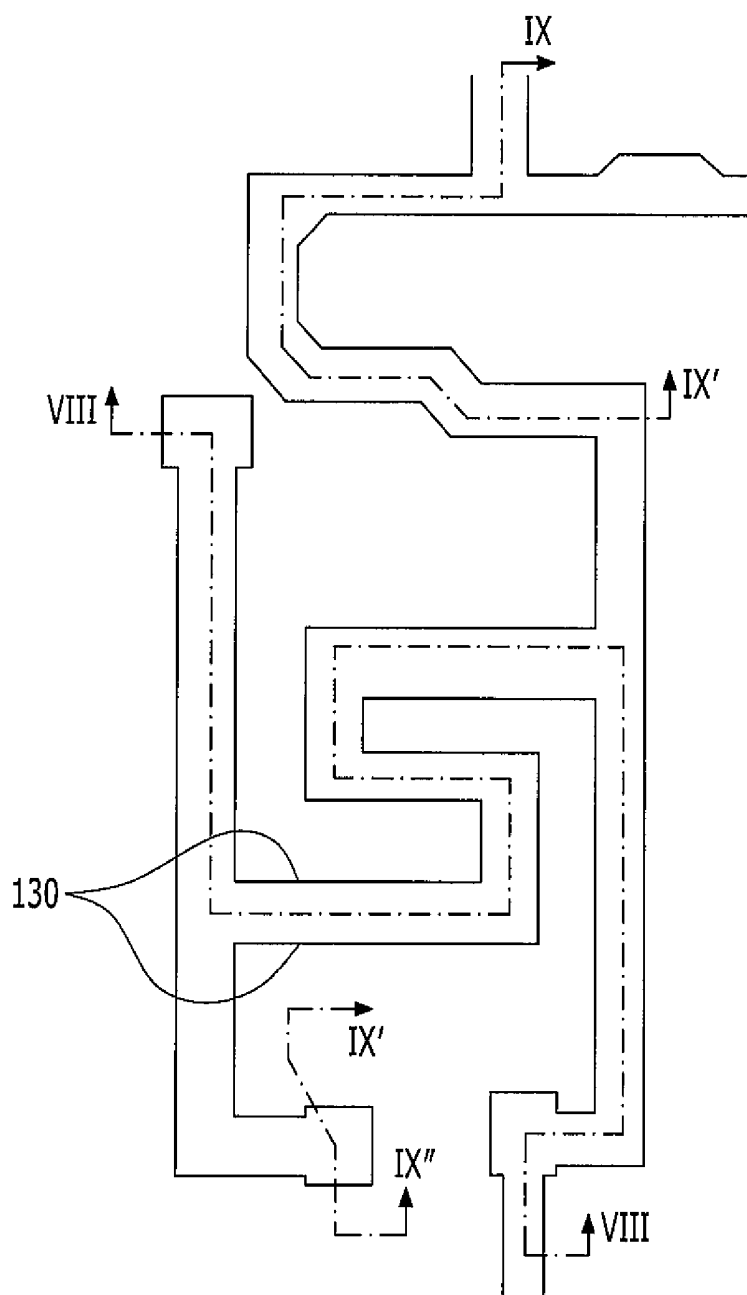


FIG. 8

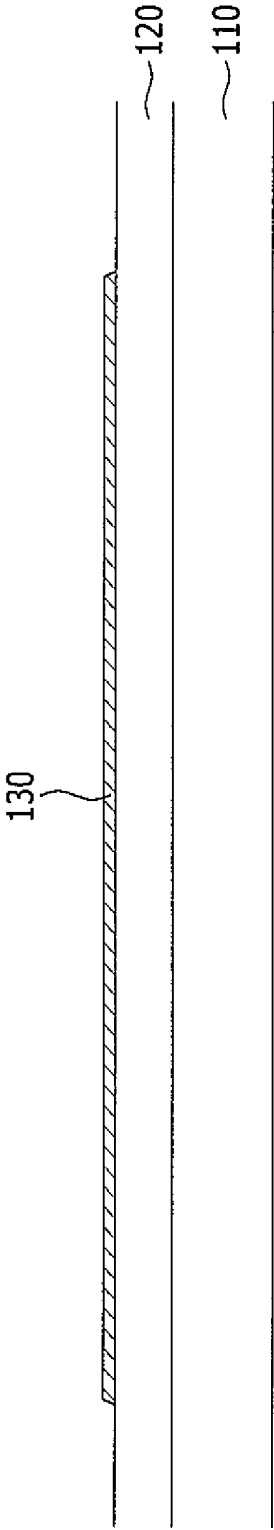


FIG. 9

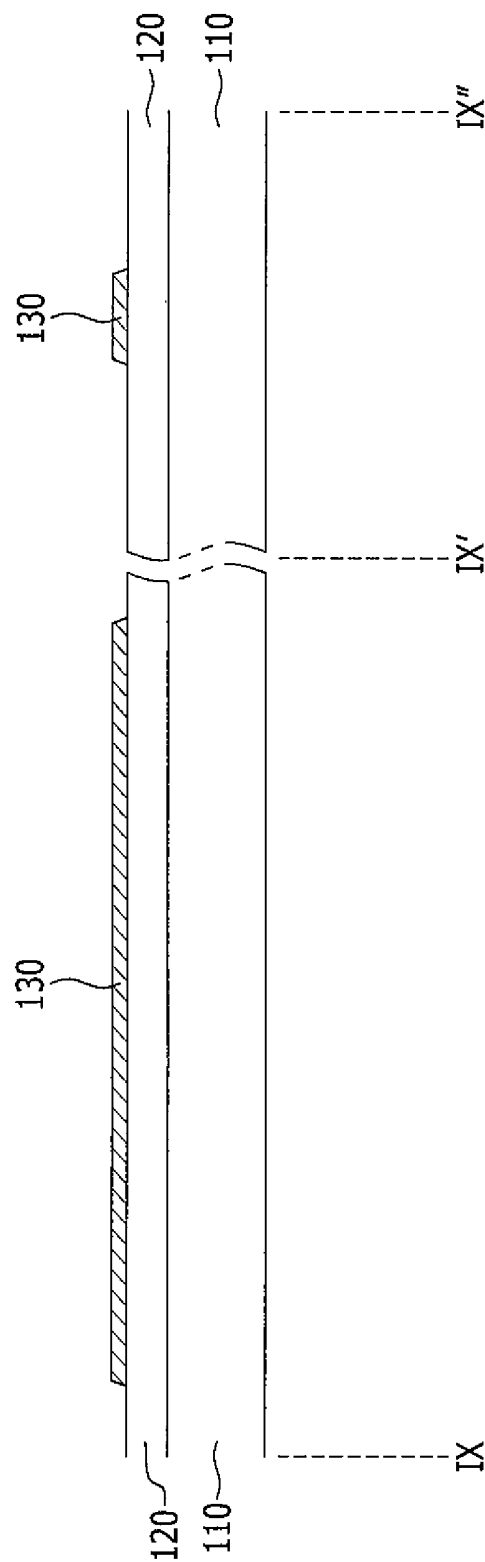


FIG. 10

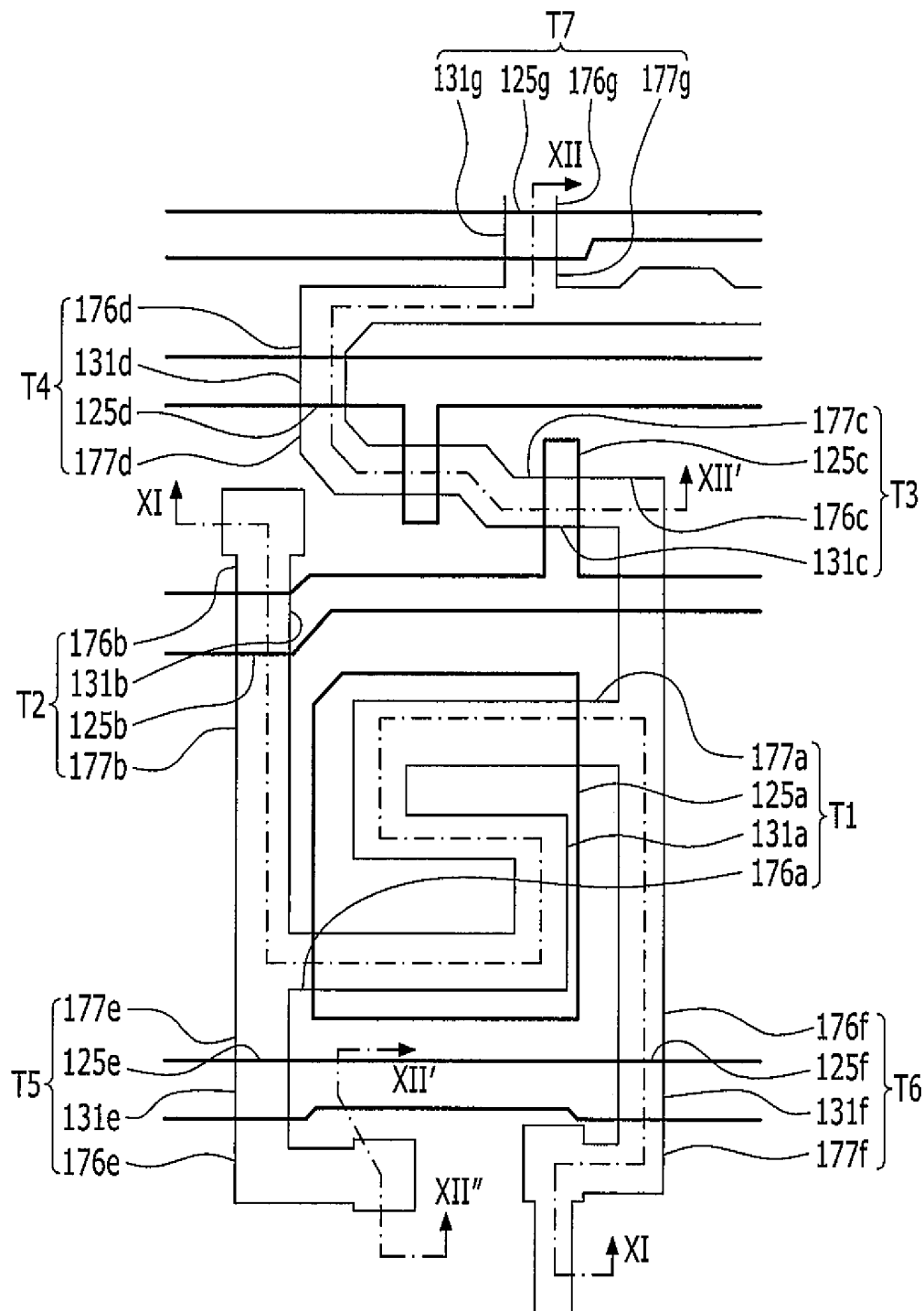


FIG. 11

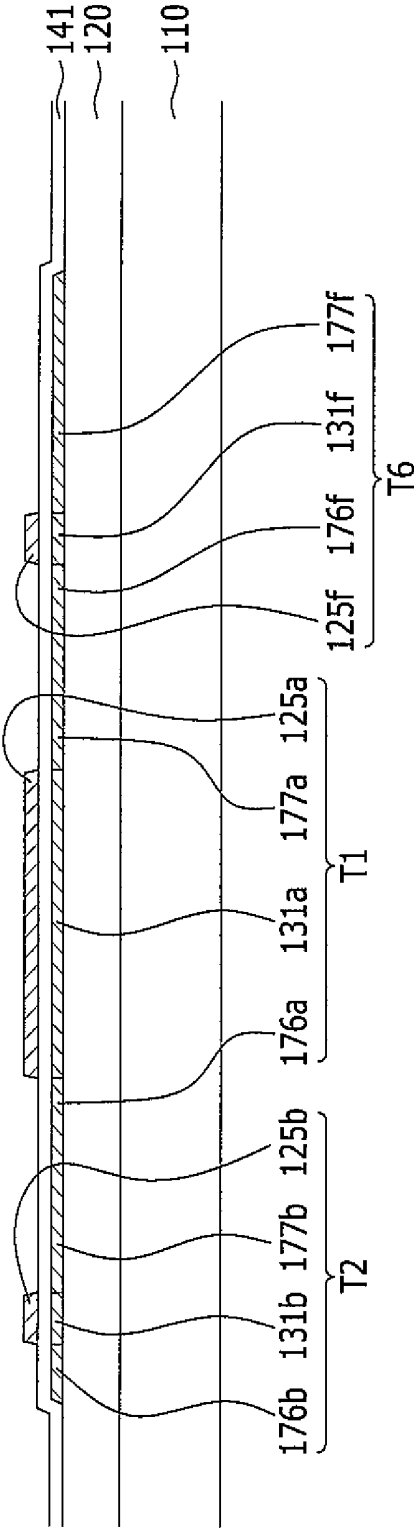


FIG. 12

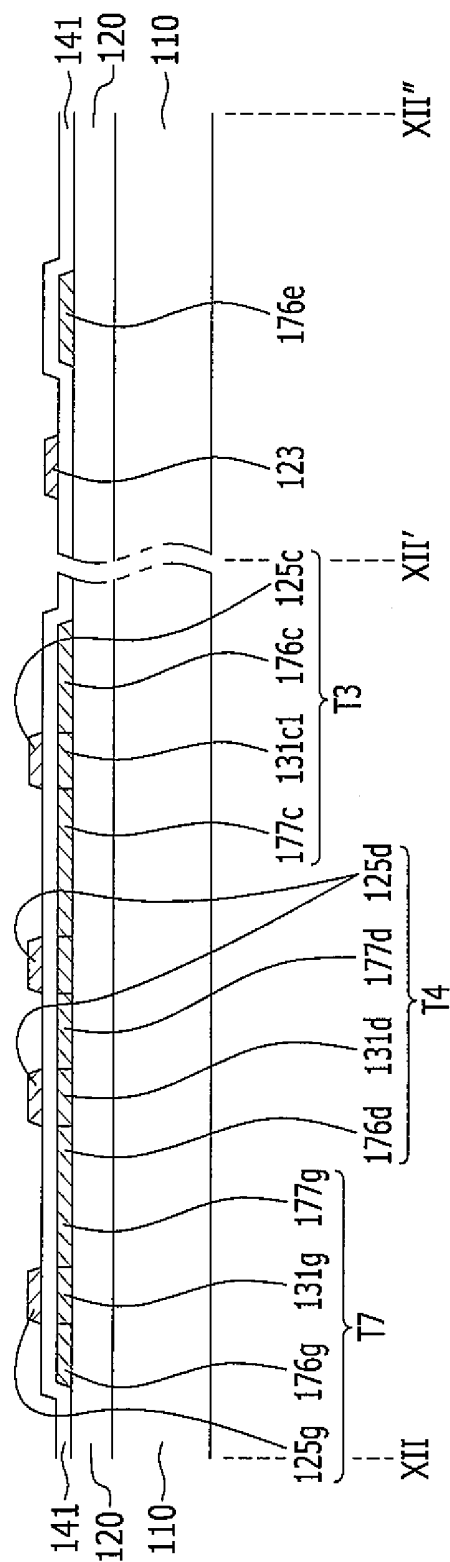


FIG. 13

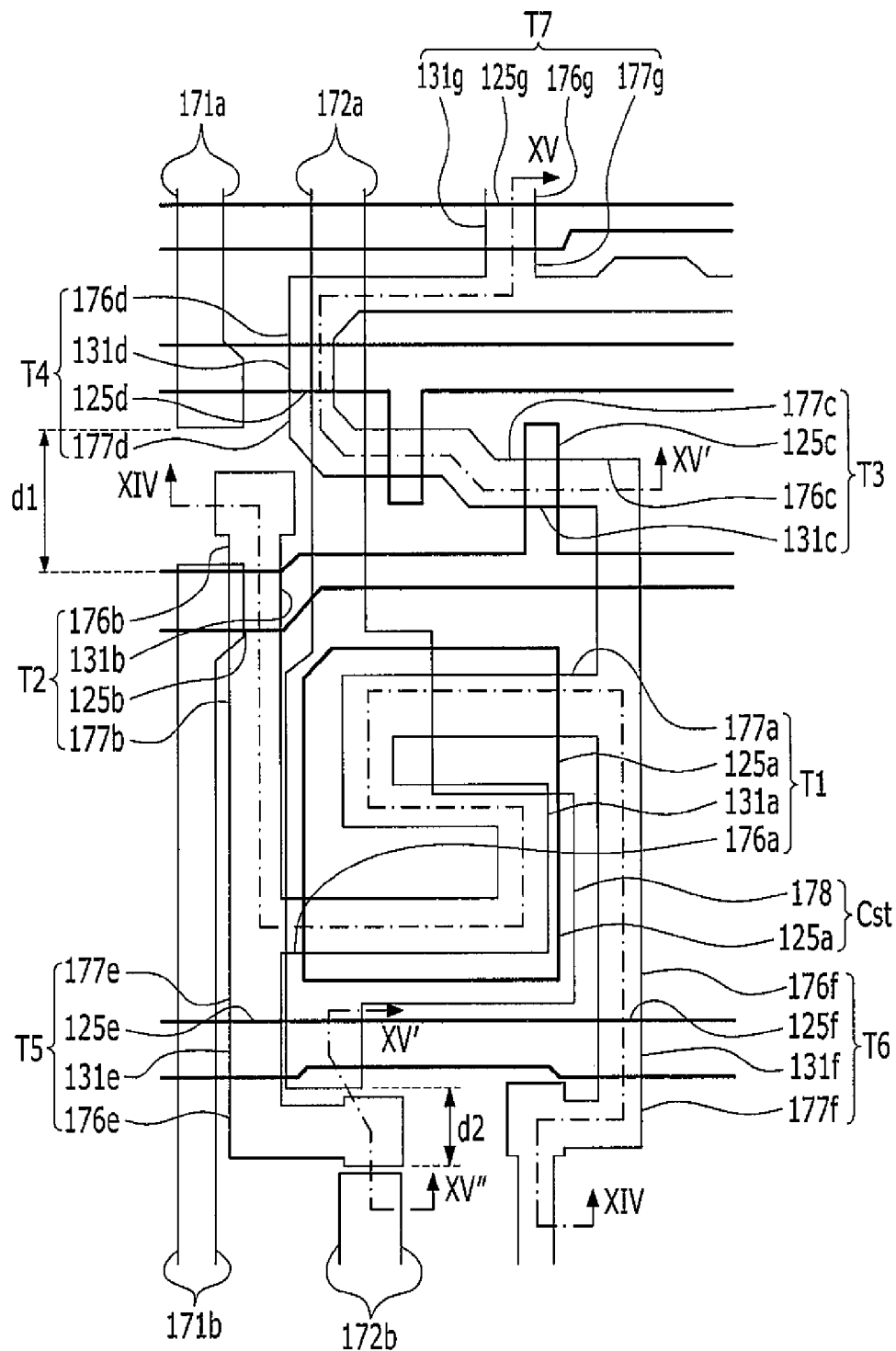


FIG. 14

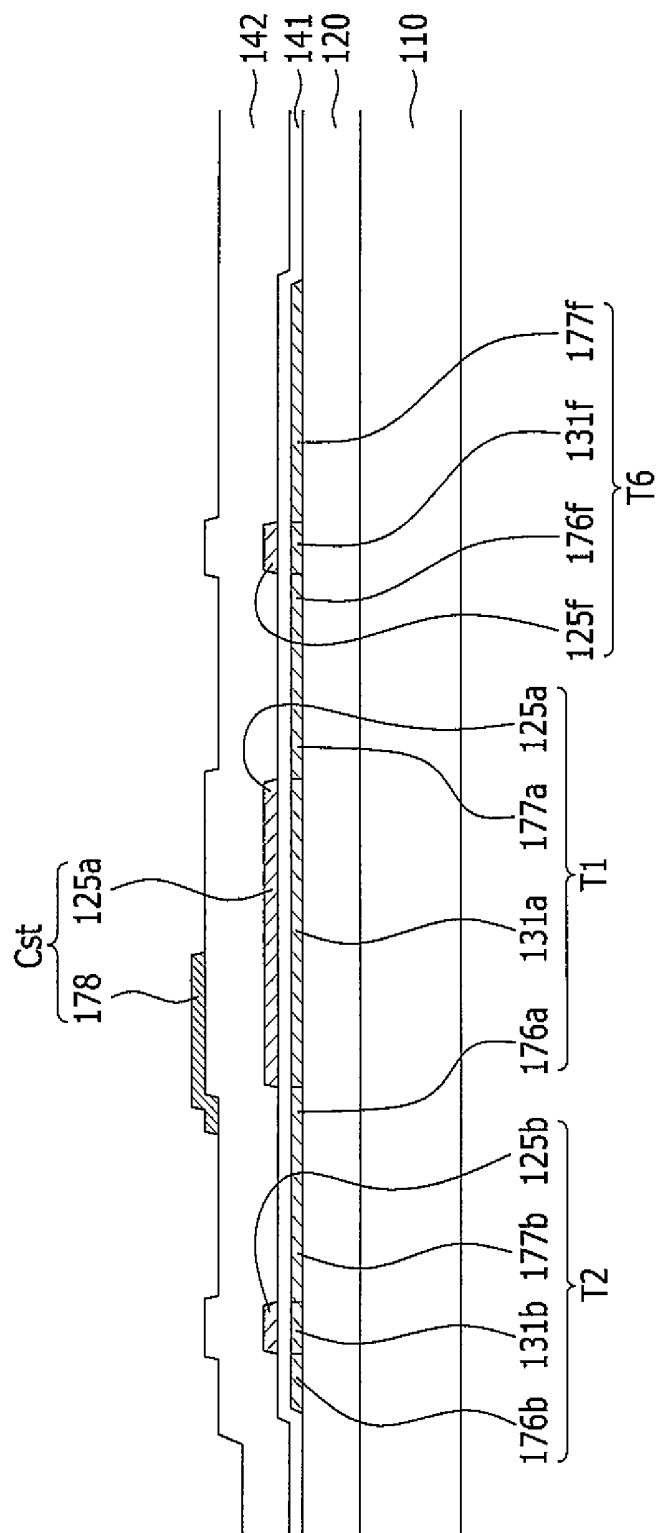
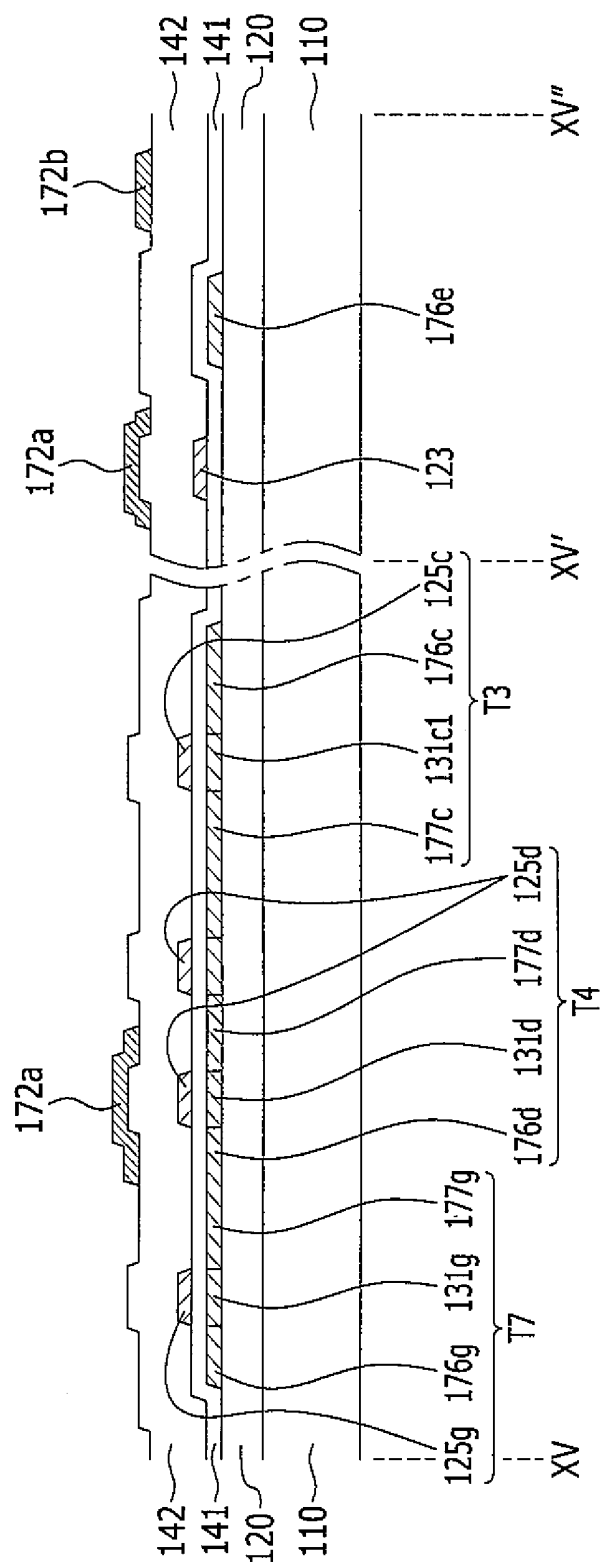


FIG. 15



ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to and the benefit of Korean Patent Application No. 10-2014-0122273 filed in the Korean Intellectual Property Office on Sep. 15, 2014, the entire contents of which are incorporated herein by reference.

BACKGROUND

1. Field

Embodiments of the present disclosure relate to an organic light emitting display device and a manufacturing method thereof.

2. Description of the Related Art

An organic light emitting diode display (i.e., an organic light emitting display device) includes two electrodes and an organic emission layer positioned therebetween, and electrons injected from one electrode and holes injected from the other electrode are coupled with each other in the organic emission layer to generate excitons, and the excitons emit energy to emit light.

An organic light emitting diode display includes a plurality of pixels including organic light emitting diodes which are self-emission devices. Each pixel also includes a plurality of thin film transistors for driving the organic light emitting diode and at least one storage capacitor. The plurality of thin film transistors include a switching thin film transistor and a driving thin film transistor.

As described, a plurality of transistors and a capacitor are formed in each pixel and organic emission layer is also formed on the transistors and the capacitor in the organic light emitting display device, and thus a lot of masks are used. However, the cost for each mask may be very high, thereby causing an increase in manufacturing cost.

The above information disclosed in this Background section is only for enhancement of understanding of the background of the present disclosure and therefore it may contain information that does not form prior art.

SUMMARY

Embodiments of the present disclosure has been made in an effort to provide an organic light emitting display device that can use at least one less mask by changing a pixel structure to thereby reduce manufacturing cost, and a manufacturing method thereof.

An organic light emitting display device according to an exemplary embodiment of the present disclosure includes: a substrate; a semiconductor on the substrate and including a switching channel of a switching transistor and a driving channel of a driving transistor, the driving transistor being spaced from the switching transistor; a first insulating layer covering the semiconductor; a switching gate electrode on the first insulating layer and overlapping the switching channel; a driving gate electrode on the first gate insulating layer and overlapping the driving channel; a second insulating layer covering the switching gate electrode and the driving gate electrode; a data line on the second insulating layer and transmitting a data signal comprising: an upper data line; and a lower data line spaced from the upper data line; a driving voltage line on the second insulating layer and

transmitting a driving voltage; a passivation layer covering the data line and the driving voltage line; a pixel electrode on the passivation layer; and a first pixel connecting member on the passivation layer and connecting the upper data line and the lower data line.

The first pixel connecting member may be connected with the upper data line and the lower data line through one or more first contact holes in the passivation layer.

The semiconductor may include a switching source electrode at a side of the switching channel and a switching drain electrode at another side of the switching channel, and the first pixel connecting member may be connected with the switching source electrode through a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

The organic light emitting display device may further include a second pixel connecting member on the passivation layer, wherein the driving voltage line may include an upper driving voltage line and a lower driving voltage line spaced from the upper driving voltage line, and the second pixel connecting member may connect the upper driving voltage line and the lower driving voltage line.

The second pixel connecting member may be connected with the upper driving voltage line and the lower driving voltage line, respectively, through a first contact hole in the passivation layer.

The organic light emitting display device may further include: a scan line connected with the switching gate electrode and transmitting a scan signal; a light emission control line in the same layer as the scan line and transmitting a light emission control signal; and an operation control transistor including an operation control gate electrode, which is a part of the light emission control line, an operation control source electrode in the semiconductor, and an operation control drain electrode in the semiconductor, wherein the second pixel connecting member may be connected with the operation control source electrode through a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

The organic light emitting display device may further include: a compensation transistor including a compensation gate electrode, which is a part of the scan line, a compensation source electrode in the semiconductor, and a compensation drain electrode in the semiconductor; and a third pixel connecting member in the same layer as the pixel electrode and connecting the driving gate electrode and the compensation drain electrode.

The third pixel connecting member may be connected with the compensation drain electrode through another second contact hole and may be connected with the driving gate electrode through a third contact hole in the second insulating layer and the passivation layer.

The organic light emitting display device may further include: a previous scan line in the same layer as the scan line and transmitting a previous scan signal; an initialization voltage line in the same layer as the pixel electrode and transmitting an initialization voltage line; and an initialization transistor including an initialization gate electrode, which is a part of the previous scan line, an initialization source electrode in the semiconductor, and an initialization drain electrode in the semiconductor, wherein the initialization voltage line may be connected with the initialization source electrode through another second contact hole.

The organic light emitting display device may further include a light emission control transistor including a light emission control gate electrode, which is a part of the light emission control line, a light emission control source elec-

trode in the semiconductor, and a light emission control drain electrode in the semiconductor, wherein the pixel electrode may be connected with the light emission control drain electrode through another second contact hole.

The organic light emitting display device may further include a storage capacitor overlapping the driving gate electrode, wherein the storage capacitor may include a first storage capacitor plate, which is the driving gate electrode; and a second storage capacitor plate overlapping the first storage capacitor plate and on the second insulating layer, and the second storage capacitor plate may be an expanded area of the upper driving voltage line.

The driving channel may include at least one curved portion.

The organic light emitting display device may further include: an organic emission layer on the pixel electrode; and a common electrode covering the organic emission layer.

According to another exemplary embodiment of the present disclosure, a method for manufacturing an organic light emitting display device includes: forming a semiconductor on a substrate; forming a first insulating layer on the semiconductor; forming a driving gate electrode of a driving transistor and a switching gate electrode of a switching transistor on the first insulating layer; forming a driving channel and a switching channel in the semiconductor provided under the driving gate electrode and the switching gate electrode by performing a doping process; forming a second insulating layer covering the driving gate electrode and the switching gate electrode; forming a data line including an upper data line and a lower data line that are spaced from each other on the second insulating layer; forming a passivation layer covering the data line; and forming a pixel electrode and a first pixel connecting member on the passivation layer, wherein the first pixel connects member connects the upper data line and the lower data line.

The method may further include: forming a contact hole in the passivation layer after forming the passivation layer; and exposing the semiconductor by etching the first insulating layer and the second insulating layer exposed in the contact hole by performing a dry etching process in the contact hole, wherein the contact hole may include a first contact hole only in the passivation layer and a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

The first pixel connecting member may be connected with the upper data line and the lower data line through the first contact hole and connected with the semiconductor through the second contact hole.

The forming the data line may include forming a driving voltage line that includes an upper driving voltage line and a lower driving voltage line spaced from the upper driving voltage line, and the forming the first pixel connecting member may include forming a second pixel connecting member that connects the upper driving voltage line and the lower driving voltage line.

The second pixel connecting member may be connected with the upper driving voltage line and the lower driving voltage line, through the first contact hole, and may be connected with the semiconductor through the second contact hole.

After forming the second insulating layer, a dopant activation process may be performed on the semiconductor to eliminate damage to an interface between the semiconductor and the insulating layer.

According to an exemplary embodiment of the present disclosure, a dry etching process is additionally performed at

the contact hole in the passivation layer such that a contact hole is formed in an inorganic layer without using an additional mask, thereby reducing the number of masks.

In addition, the second storage capacitor plate is formed of the same or substantially the same material in the same layer as the driving voltage line and the data line so that at least one mask can be eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an equivalent circuit diagram of an organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 2 is a timing diagram of a signal applied to one pixel of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 3 schematically illustrates a plurality of transistors and a capacitor of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 4 is a detailed layout view of FIG. 3.

FIG. 5 is a cross-sectional view of the organic light emitting display device of FIG. 4, taken along the line V-V.

FIG. 6 is a cross-sectional view of the organic light emitting display device of FIG. 4, taken along the line VI-VI' and VI'-VI''.

FIG. 7 is a layout view of a manufacturing method of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 8 is a cross-sectional view of the organic light emitting display device of FIG. 7, taken along the line VIII-VIII'.

FIG. 9 is a cross-sectional view of the organic light emitting display device of FIG. 7, taken along the lines IX-IX' and IX'-IX''.

FIG. 10 is a layout view of a manufacturing method of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 11 is a cross-sectional view of the organic light emitting display device of FIG. 10, taken along the line XI-XI'.

FIG. 12 is a cross-sectional view of the organic light emitting display device of FIG. 10, taken along the lines XII-XII' and XII'-XII''.

FIG. 13 is a layout view of a manufacturing method of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

FIG. 14 is a cross-sectional view of the organic light emitting display device of FIG. 13, taken along the line XIV-XIV'.

FIG. 15 is a cross-sectional view of the organic light emitting display device of FIG. 13, taken along the lines XV-XV' and XV'-XV''.

DETAILED DESCRIPTION

Embodiments of the present disclosure will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the disclosure are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

The drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification.

Further, the size and thickness of each configuration shown in the drawings are arbitrarily shown for better understanding and ease of description, but the present disclosure is not limited thereto.

In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. In the drawings, for better understanding and ease of description, the thickness of some layers and areas is exaggerated. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present.

In addition, unless explicitly described to the contrary, the words “comprise” and “includes” and variations such as “comprises,” “comprising,” “includes,” and “including” will be understood to imply the inclusion of stated elements but not the exclusion of any other elements. Further, in the specification, the word “on” means positioning on or below the object portion, and does not essentially mean positioning on the upper side of the object portion based on a gravity direction.

Further, in this specification, the word “on a plane” means viewing a target portion from the top, and the word “on a cross-section” means viewing a cross-section formed by vertically cutting a target portion from the side.

Spatially relative terms, such as “beneath,” “below,” “lower,” “under,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or in operation, in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below” or “beneath” or “under” other elements or features would then be oriented “above” the other elements or features. Thus, the example terms “below” and “under” can encompass both an orientation of above and below. The device may be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein should be interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being “between” two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the inventive concept. As used herein, the singular forms “a” and “an” are intended to include the plural forms as well, unless the context clearly indicates otherwise.

Expressions such as “at least one of,” when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. Further, the use of “may” when describing embodiments of the inventive concept refers to “one or more embodiments of the inventive concept.” Also, the term “exemplary” is intended to refer to an example or illustration.

It will be understood that when an element or layer is referred to as being “on,” “connected to,” “coupled to,” “connected with,” “coupled with,” or “adjacent to” another element or layer, it can be directly on, connected to, coupled to, connected with, coupled with, or adjacent to the other element or layer, or one or more intervening elements or layers may be present. In contrast, when an element or layer is referred to as being “directly on,” “directly connected to,” “directly coupled to,” “directly connected with,” “directly

coupled with,” or “immediately adjacent to” another element or layer, there are no intervening elements or layers present.

As used herein, the term “substantially,” “about,” and similar terms are used as terms of approximation and not as terms of degree, and are intended to account for the inherent deviations in measured or calculated values that would be recognized by those of ordinary skill in the art.

As used herein, the terms “use,” “using,” and “used” may be considered synonymous with the terms “utilize,” “utilizing,” and “utilized,” respectively.

The organic light emitting display device and/or any other relevant devices or components according to embodiments of the present invention described herein may be implemented utilizing any suitable hardware, firmware (e.g. an application-specific integrated circuit), software, or a suitable combination of software, firmware, and hardware. For example, the various components of the organic light emitting display device may be formed on one integrated circuit (IC) chip or on separate IC chips. Further, the various components of the organic light emitting display device may be implemented on a flexible printed circuit film, a tape carrier package (TCP), a printed circuit board (PCB), or formed on a same substrate as the organic light emitting display device. Further, the various components of the organic light emitting display device may be a process or thread, running on one or more processors, in one or more computing devices, executing computer program instructions and interacting with other system components for performing the various functionalities described herein. The computer program instructions are stored in a memory which may be implemented in a computing device using a standard memory device, such as, for example, a random access memory (RAM). The computer program instructions may also be stored in other non-transitory computer readable media such as, for example, a CD-ROM, flash drive, or the like. Also, a person of skill in the art should recognize that the functionality of various computing devices may be combined or integrated into a single computing device, or the functionality of a particular computing device may be distributed across one or more other computing devices without departing from the scope of an exemplary embodiments of the present invention.

An organic light emitting display device according to an exemplary embodiment of the present disclosure will be described with reference to FIG. 1 through FIG. 6.

FIG. 1 is an equivalent circuit diagram of one pixel of the organic light emitting display device according to an exemplary embodiment of the present disclosure.

As shown in FIG. 1, one pixel 1 of the organic light emitting display device according to an exemplary embodiment of the present disclosure includes a plurality of signal lines 121, 122, 123, 128, 171, 172, and 192, a plurality of transistors T1, T2, T3, T4, T5, T6, and T7 connected to the plurality of signal lines, a storage capacitor Cst, and an organic light emitting diode OLED.

The transistors T1, T2, T3, T4, T5, T6, and T7 include a driving transistor T1, a switching transistor T2, a compensation transistor T3, an initialization transistor T4, an operation control transistor T5, a light emission control transistor T6, and a bypass transistor T7.

The signal lines 121, 122, 123, 128, 171, 172, and 192 include a scan line 121 transmitting a scan signal Sn, a previous scan line 122 transmitting a previous scan signal Sn-1, an emission control line 123 transmitting an emission control signal EM to the operation control transistor T5 and the light emission control transistor T6, a bypass control line

128 transmitting a bypass signal BP to the bypass transistor T7, a data line 171 crossing the scan line 121 and transmitting a data signal Dm, a driving voltage line 172 crossing the scan line 121 and formed almost (e.g., substantially) in parallel with the data line 171, and an initialization voltage line 192 transmitting an initialization voltage Vint that initializes the driving transistor T1.

A gate electrode G1 of the driving transistor T1 is connected with one end Cst1 of the storage capacitor Cst, a source electrode S1 of the driving transistor T1 is connected with the driving voltage line 172 via the operation control transistor T5, and a drain electrode D1 of the driving transistor T1 is electrically connected with an anode of the organic light emitting diode OLED via the light emission control transistor T6. The driving transistor T1 receives the data signal Dm and transmits a driving current Id to the organic light emitting diode OLED according to a switching operation of the switching transistor T2.

A gate electrode G2 of the switching transistor T2 is connected with the scan line 121, a source electrode S2 of the switching transistor T2 is connected with the data line 171, and a drain electrode D2 of the switching transistor T2 is connected with the source electrode S1 of the driving transistor T1 and is connected with the driving voltage line 172 via the operation control transistor T5. Such a switching transistor T2 is turned on by a scan signal Sn transmitted through the scan line 121, and performs a switching operation for transmission of a data signal Dm transmitted to the data line 171 to the source electrode S1 of the driving transistor T1.

A gate electrode G3 of the compensation transistor T3 is connected to the scan line 121, a source electrode S3 of the compensation transistor T3 is connected with the drain electrode D1 of the driving transistor T1 and connected with an anode of the organic light emitting diode OLED via the light emission control transistor T6, and a drain electrode D3 of the compensation transistor T3 is connected to a drain electrode D4 of the initialization transistor T4, a first end Cst1 of the storage capacitor Cst, and the gate electrode g1 of the driving transistor T1. Such a compensation transistor T3 is turned on according to the scan signal Sn transmitted through the scan line 121, and diode-connects the driving transistor T1 by connecting the gate electrode G1 and the drain electrode D1 of the driving transistor T1 to each other.

A gate electrode G4 of the initialization transistor T4 is connected with the previous scan line 122, a source electrode S4 of the initialization transistor T4 is connected with the initialization voltage line 192, and a drain electrode D4 of the initialization transistor T4 is connected with the first end Cst1 of the storage capacitor Cst and the gate electrode G1 of the driving transistor T1 through the drain electrode D3 of the compensation transistor T3. Such an initialization transistor T4 is turned on according to the previous scan signal Sn-1 transmitted through the previous scan line 122, and performs an initialization operation for initialization of a gate voltage of the gate electrode G1 of the driving transistor T1 by transmitting the initialization voltage Vint to the gate electrode G1 of the driving transistor T1.

A gate electrode G5 of the operation control transistor T5 is connected with a light emission control line 123, a source electrode S5 of operation control transistor T5 is connected with the driving voltage line 172, and a drain electrode D5 of the operation control transistor T5 is connected with the source electrode S1 of the driving transistor T1 and the drain electrode S2 of the switching transistor T2.

A gate electrode G6 of the light emission control transistor T6 is connected with the light emission control line 123,

a source electrode S6 of the light emission control transistor T6 is connected with the drain electrode D1 of the driving transistor T1 and the source electrode S3 of the compensation transistor T3, and a drain electrode D6 of the light emission control transistor T6 is electrically connected with the anode of the organic light emitting diode OLED. The operation control transistor T5 and the light emission control transistor T6 are concurrently (e.g., simultaneously) turned on according to a light emission control signal EM transmitted through the light emission control line 123 such that the driving voltage ELVDD is compensated through the diode-connected driving transistor T1 and thus transmitted to the organic light emitting diode OLED.

A gate electrode G7 of the bypass transistor T7 is connected with a bypass control line 128, a source electrode S7 of the bypass transistor T7 is connected with the drain electrode D6 of the light emission control transistor T6 and the anode of the organic light emitting diode OLED, and a drain electrode D7 of the bypass transistor T7 is connected with the initialization voltage line 192 and the source electrode S4 of the initialization transistor T4.

A second end Cst2 of the storage capacitor Cst is connected with the driving voltage line 172, and a cathode of the organic light emitting diode OLED is connected with a common voltage line 741 that transmits a common voltage ELVSS.

Hereinafter, an operation process of one pixel of the organic light emitting display device according to an exemplary embodiment of the present disclosure will be described in detail with reference to FIG. 2.

First, a low-level previous scan signal Sn-1 is supplied through the previous scan line 122 during an initialization period. The initialization transistor T4 is turned on corresponding to the low-level previous scan signal Sn-1, and the initialization voltage Vint is connected to the gate electrode G1 of the driving transistor T1 through the initialization transistor T4 such that the driving transistor T1 is initialized through the initialization voltage Vint.

Next, a low-level scan signal Sn is supplied through the scan line 121 during a data programming period. The switching transistor T2 and the compensation transistor T3 are turned on corresponding to the low-level scan signal Sn. The driving transistor T1 is diode-connected by the turned-on compensation transistor T3 and thus biased in a forward direction.

Then, a compensation voltage $Dm + V_{th}$ (V_{th} is a negative (-) value), reduced by a threshold voltage V_{th} of the driving transistor T1 from the data signal Dm supplied from the data line 171, is applied to the gate electrode G1 of the driving transistor T1. The driving voltage ELVDD and a compensation voltage ($Dm + V_{th}$) are applied to both ends of the storage capacitor Cst, and a charge corresponding to a voltage difference between both ends is stored in the storage capacitor Cst.

After that, the light emission control signal EM supplied from the light emission control line 123 is changed to a low level from a high level during a light emission period. The operation control transistor T5 and the light emission control transistor T6 are turned on by the low-level light emission control signal EM during the light emission period.

A driving current Id is generated according to a voltage difference between the voltage of the gate electrode G1 of the driving transistor T1 and the driving voltage ELVDD, and the driving current Id is supplied to the organic light emitting diode OLED through the emission control transistor T6. A gate-source voltage V_{gs} of the driving transistor T1 is maintained at $(Dm + V_{th}) - ELVDD$ by the storage capaci-

tor Cst during the light emission period, and the driving current I_d is proportional to the square $(D_m - ELVDD)^2$ of a value obtained by subtracting the threshold voltage from the source-gate voltage V_{gs} according to a current-voltage relationship of the driving transistor T1. Thus, the driving current I_d is determined regardless of the threshold voltage V_{th} of the driving transistor T1.

The bypass transistor T7 receives a bypass signal BP from the bypass control line 128. The bypass signal BP is a voltage having a level (e.g., a predetermined level) which always turns off the bypass transistor T7, the bypass transistor T7 receives a voltage having a transistor-off level from the gate electrode G7, and thus the bypass transistor T7 is always turned off, and a part of the driving current I_d flows out through the bypass thin film transistor T7 as a bypass current I_{bp} in the off state.

Although a small (e.g., minimum) current may flow through the driving transistor T1 as a driving current, a black image cannot be properly displayed if the organic light emitting diode OLED emits light. Thus, the bypass transistor T7 of the organic light emitting display device according to an exemplary embodiment of the present disclosure may disperse a part of the small (e.g., minimum) current of the driving transistor T1 to current paths other than a current path toward the organic light emitting diode OLED as a bypass current I_{bp} . Here, the small (e.g., minimum) current of the driving transistor T1 implies a current under a condition that the transistor T1 is turned off because the gate-source voltage V_{gs} of the driving transistor T1 is lower than the threshold voltage V_{th} . A small (e.g., minimum) driving current (e.g., a current lower than 10 pA) under the condition that turns off the driving transistor T1 is transmitted to the organic light emitting diode OLED such that an image is displayed with black luminance. When the small (e.g., minimum) driving current that displays the black image flows, an influence of bypass transmission of the bypass current I_{bp} is high, but when a high driving current that displays an image such as a general image or a white image flows, the bypass current I_{bp} has almost (e.g., substantially) no influence. Thus, when the driving current displaying the black image flows, a light emission current baled reduced by an amount of current the bypass current I_{bp} leaked through the bypass transistor T7 from the driving current I_d has a lower amount of current for clear representation of the black image. Therefore, an image having precise black luminance can be realized using the bypass transistor T7, thereby improving a contrast ratio. In FIG. 2, the bypass signal BP is equivalent to the previous scan signal S_{n-1} , but this is not restrictive. In addition, in an exemplary embodiment of the present disclosure, a seven transistor-one

transistor structure is illustrated, but the present disclosure is not limited thereto.

Now, a detailed structure of the pixel of the organic light emitting display device shown in FIG. 1 will be described in detail with reference to FIG. 3 through FIG. 6, together with FIG. 1.

FIG. 3 is a schematic diagram of the plurality of transistors and capacitors of the organic light emitting display device according to an exemplary embodiment of the present disclosure, FIG. 4 is a detailed layout view of FIG. 3, FIG. 5 is a cross-sectional view of the organic light emitting display device shown in FIG. 4, taken along the line V-V, and FIG. 6 is a cross-sectional view of the organic light emitting display device of FIG. 4, taken along the line VI-VI.

Hereinafter, a detailed planar structure of the organic light emitting diode display according to an exemplary embodi-

ment of the present disclosure will be first described in detail with reference to FIGS. 3 and 4, and then a detailed cross-sectional structure will be described in detail with reference to FIG. 5 and FIG. 6.

First, as shown in FIG. 3, the organic light emitting display device according to an exemplary embodiment of the present disclosure includes the scan line 121, the previous scan line 122, the light emission control line 123, and the bypass control line 128 respectively applying the scan signal S_n , the previous scan signal S_{n-1} , the light emission control signal EM, and the bypass signal BP. The lines 121, 122, 123, and 128 each extend in a row direction. The organic light emitting display device according to an exemplary embodiment of the present disclosure further includes the data line 171 and the driving voltage line 172 crossing the scan line 121, the previous scan line 122, the light emission control line 123, and the bypass control line 128. The data line 171 and the driving voltage line 172 respectively apply the data signal D_m and the driving voltage ELVDD to the pixel. The initialization voltage V_{int} is transmitted to the compensation transistor T3 through the initialization voltage line 192. When viewed on a plane, the data line 171 includes an upper data line 171a spaced from the data line 171 and provided in an upper portion in the pixel and a lower data line 171b spaced from the upper data line 171a by a distance (e.g., a predetermined distance) d_1 and provided in a lower portion in the pixel. When viewed on a plane, the driving voltage line 172 includes an upper driving voltage line 172a provided in an upper portion in the pixel and a lower driving voltage line 172b spaced from the upper driving voltage line 172a by a distance (e.g., a predetermined distance) d_2 and provided in a lower portion in the pixel.

In addition, an organic light emitting diode OLED including a pixel electrode 191, an organic emission layer 370, and a common electrode 270, is formed on the driving transistor T1, the switching transistor T2, the compensation transistor T3, the initialization transistor T4, the operation control transistor T5, the light emission control transistor T6, the bypass transistor T7, the storage capacitor Cst, in the pixel.

Each channel of the driving transistor T1, the switching transistor T2, the compensation transistor T3, the initialization transistor T4, the operation control transistor T5, the light emission control transistor T6, and the bypass transistor T7 is formed in one semiconductor 130 connected thereto, and the semiconductor 130 is formed by being curved in various shapes. Such a semiconductor 130 may be formed of a polycrystalline material or an oxide semiconductor material. The oxide semiconductor material may include one of titanium (Ti), hafnium (Hf), zirconium (Zr), aluminum (Al), tantalum (Ta), germanium (Ge), zinc (Zn), gallium (Ga), tin (Sn), or indium (In), or zinc oxide (ZnO), indium-gallium-zinc oxide (InGaZnO4), indium-zinc oxide (Zn—In—O), zinc-tin oxide (Zn—Sn—O), indium-gallium oxide (In—Ga—O), indium-tin oxide (In—Sn—O), indium-zirconium oxide (In—Zr—O), indium-zirconium-zinc oxide (In—Zr—Zn—O), indium-zirconium-tin oxide (In—Zr—Sn—O), indium-zirconium-gallium oxide (In—Zr—Ga—O), indium-aluminum oxide (In—Al—O), indium-zinc-aluminum oxide (In—Zn—Al—O), indium-tin-aluminum oxide (In—Sn—Al—O), indium-aluminum-gallium oxide (In—Al—Ga—O), indium-tantalum oxide (In—Ta—O), indium-tantalum-zinc oxide (In—Ta—Zn—O), indium-tantalum-tin oxide (In—Ta—Sn—O), indium-tantalum-gallium oxide (In—Ta—Ga—O), indium-germanium oxide (In—Ge—O), indium-germanium-zinc oxide (In—Ge—Zn—O), indium-germanium-tin oxide (In—Ge—Sn—O), indium-germanium-gallium oxide (In—Ge—Ga—O), titanium-indium-

zinc oxide (Ti—In—Zn—O), and hafnium-indium-zinc oxide (Hf—In—Zn—O), which are complex oxides thereof. When the semiconductor **130** is formed of the oxide semiconductor material, an additional protection layer may be provided for protection of the oxide semiconductor material that is weak to an external environment such as a high temperature and the like.

The semiconductor **130** includes a channel region in which a channel is doped with an N-type impurity or a P-type impurity, and a source region and a drain region, which are formed at both sides of the channel region and formed by doping the doping impurity which is an opposite type to the doping impurity doped in the channel region. In the present exemplary embodiment, the source doping region and the drain doping region respectively correspond to a source electrode and a drain electrode. The source electrode and the drain electrode formed in the semiconductor **130** may be formed by doping only the corresponding regions. In addition, a source electrode and a drain electrode in a region between a source electrode and a drain electrode of different transistors may be electrically connected to each other.

As shown in FIG. 4, a channel **131** includes a driving channel **131a** formed in the driving transistor **T1**, a switching channel **131b** formed in the switching transistor **T2**, a compensation channel **131c** formed in the compensation transistor **T3**, an initialization channel **131d** formed in the initialization transistor **T4**, an operation control channel **131e** formed in the operation control transistor **T5**, a light emission control channel **131f** formed in the light emission control transistor **T6**, and a bypass channel **131g** formed in the bypass transistor **T7**.

The driving transistor **T1** includes the driving channel **131a**, a driving gate electrode **125a**, a driving source electrode **176a**, and a driving drain electrode **177a**. The driving channel **131a** is curved and may have an oblique shape or a zigzag shape. As such, the curved driving semiconductor layer **131a** is formed, and thus the driving semiconductor layer **131a** may be elongated in a narrow space. Thus, a driving range of a gate voltage applied to the driving gate electrode **125a** is widened by the elongated driving channel **131a**. Accordingly, since the driving range of a gate voltage is increased, a gray level of light emitted from the organic light emitting diode OLED may be more finely controlled by changing a magnitude of the gate voltage, thereby enhancing resolution of the organic light emitting diode display and improving display quality. The shape of such a driving semiconductor layer **131a** is variously modified, and thus various exemplary embodiments such as 'reverse S', 'S', 'M', 'W', and the like are possible.

The driving gate electrode **125a** overlaps the driving channel **131a**, and the driving gate electrode **125a** is formed in the same layer with the same or substantially the same material as the scan line **121**, the previous scan line **122**, the emission control line **123**, a switching gate electrode **125b**, a compensation gate electrode **125c**, an initialization gate electrode **125d**, an operation control gate electrode **125e**, and an emission control gate electrode **125f**. The driving source electrode **176a** and the driving drain electrode **177a** do not overlap the driving channel **131a**.

The switching transistor **T2** includes the switching channel **131b**, the switching gate electrode **125b**, a switching source electrode **176b**, and a switching drain electrode **177b**. The switching gate electrode **125b**, which is a part expanded from the scan line **121**, overlaps the switching channel **131b**, and the switching source electrode **176b** and the switching drain electrode **177b** do not overlap the switching channel

131b. The switching source electrode **176b** is connected with a first pixel connecting member **193** through a contact hole **84**.

The compensation transistor **T3** includes the compensation channel **131c**, the compensation gate electrode **125c**, a compensation source electrode **176c**, and a compensation drain electrode **177c**. The compensation gate electrode **125c**, which is a part expanded by protruding upward from the scan line **121**, overlaps the compensation channel **131c**, and the compensation source electrode **176c** and the compensation drain electrode **177c** do not overlap the compensation channel **131c**. The compensation drain electrode **177c** is connected with a third pixel connecting member **194** through a contact hole **83**.

The initialization transistor **T4** includes the initialization channel **131d**, the initialization gate electrode **125d**, an initialization source electrode **176d**, and an initialization drain electrode **177d**. Two initialization gate electrodes **125d**, each of which is a part of the previous scan line **122**, are provided for prevention or reduction of a leakage current, and overlap the initialization channel **131d**. The initialization source electrode **176d** and the initialization drain electrode **177d** do not overlap the initialization channel **131d**. The initialization source electrode **176d** is connected with the initialization voltage line **192** through a contact hole **82**.

The operation control transistor **T5** includes the operation control channel **131e**, the operation control gate electrode **125e**, an operation control source electrode **176e**, and an operation control drain electrode **177e**. The operation control gate electrode **125e**, which is a part of the light emission control line **123**, overlaps the operation control channel **131e**, and does not overlap the operation control source electrode **176e** and the operation control drain electrode **177e**. The operation control source electrode **176e** is connected with a second pixel connecting member **195** through a contact hole **85**.

The light emission control transistor **T6** includes the light emission control channel **131f**, the light emission gate electrode **125f**, a light emission source electrode **176f**, and a light emission drain electrode **177f**. The light emission gate electrode **125f**, which is a part of the light emission control line **123**, overlaps the light emission control channel **131f** and does not overlap the light emission source electrode **176f** and the light emission drain electrode **177f**. The light emission drain electrode **177f** is connected with a pixel electrode **191** through a contact hole **81**.

The bypass thin film transistor **T7** includes the bypass channel **131g**, a bypass gate electrode **125g**, a bypass source electrode **176g**, and a bypass drain electrode **177g**. The bypass gate electrode **125g**, which is a part of the bypass control line **128**, overlaps the bypass channel **131g** and does not overlap the bypass source electrode **176g** and the bypass drain electrode **177g**. The bypass source electrode **176g** is directly connected with the light emission drain electrode **177f**, and the bypass drain electrode **177g** is directly connected with the initialization source electrode **176d**.

A first end of the driving channel **131a** of the driving transistor **T1** is connected with the switching drain electrode **177b** and the operation control drain electrode **177e**, and a second end of the driving channel **131a** is connected with the compensation source electrode **176c** and the light emission source electrode **176f**.

The storage capacitor **Cst** includes the first storage capacitor plate **125a** and a second storage capacitor plate **178**, with a second insulating layer **142** interposed therebetween. The first storage capacitor plate **125a** corresponds to the driving

gate electrode **125a**, and the second storage capacitor plate **178** is an expansion area of the first driving voltage line **172a** and is formed in each pixel. Here, the second insulating layer **142** is a dielectric material, and charges stored in the capacitor Cst and a voltage between the two plates **125a** and **178** determine storage capacitance. As described, the driving gate electrode **125a** is used as the first storage capacitor plate **125a** so that a space for forming the storage capacitor can be assured in a space that is reduced due to the driving channel **131a** that occupies a large area in the pixel.

The first storage capacitor plate **125a**, which is the driving gate electrode **125a** is connected with the third pixel connecting member **194** through a contact hole **61** formed in the first insulating layer **141** and the second insulating layer **142**. The third pixel connecting member **194** is formed in the same layer as the pixel electrode **191**, and connects the driving gate electrode **125a** and the compensation drain electrode **177c** of the compensation transistor T3.

Thus, the storage capacitor Cst stores a storage capacitance that corresponds to a difference between the driving voltage ELVDD transmitted to the second storage capacitor plate **178** through the upper driving voltage line **172a** and a gate voltage of the driving gate electrode **125a**.

The data line **171** is divided into the upper data line **171a** and the lower data line **171b**, the upper data line **171a** and the lower data line **171b** are respectively connected with a first end and a second end of the first pixel connecting member **193** through the contact holes **62** and **63**, and a center portion of the first pixel connecting member **193** is directly connected with the switching source electrode **176b** through the contact hole **84**. In addition, the driving voltage line **172** is divided into the upper driving voltage line **172a** and the lower driving voltage line **172b**, the upper driving voltage line **172a** and the lower driving voltage line **172b** are respectively connected with a first end and a second end of the second pixel connecting member **195** through the contact holes **64** and **65**, and a center portion of the second pixel connecting member **195** is directly connected with the operation control source electrode **176e** through the contact hole **85**.

Hereinafter, a cross-sectional structure of the organic light emitting diode display according to an exemplary embodiment of the present disclosure will be described in detail in the order of laminating with reference to FIG. 5 and FIG. 6.

A lamination structure of the operation control transistor T5 is almost (e.g., substantially) the same as that of the light emission control transistor T6, and therefore description thereof will be omitted.

A buffer layer **120** may be formed on a substrate **110**. The substrate **110** may be formed of an insulation substrate made of an insulation material such as glass, quartz, ceramic, plastic, and the like, and the buffer layer **120** blocks an impurity from accessing the substrate **110** during a crystallization process for forming a polycrystalline semiconductor to improve a feature of the polycrystalline semiconductor, and may reduce stress applied to the substrate **110**.

The semiconductor **130** including the driving channel **131a**, the switching channel **131b**, the compensation channel **131c**, the initialization channel **131d**, the operation control channel **131e**, and the light emission control channel **131f** is formed on the buffer layer **120**. The driving source electrode **176a** and the driving drain electrode **177a** are provided at both sides of the driving channel **131a**, the switching source electrode **176b** and the switching drain electrode **177b** are provided at both sides of the switching channel **131b**, the compensation source electrode **176c** and the compensation drain electrode **177c** are provided at both sides of the com-

pensation channel **131c**, the initialization source electrode **176d** and the initialization drain electrode **177d** are provided at both sides of the initialization channel **131d**, the operation control source electrode **176e** and the operation control drain electrode **177e** are provided at both sides of the operation control channel **131e**, and the light emission source electrode **176f** and the light emission drain electrode **177f** are provided at both sides of the light emission control channel **131f**.

A first insulating layer **141** is formed to cover the semiconductor **130**. The scan line **121** including the switching gate electrode **125b** and the compensation gate electrode **125**, the previous scan line **122** including the initialization gate electrode **125d**, the light emission control line **123** including the operation control gate electrode **125e** and the light emission control gate electrode **125f**, and gate wires **121**, **122**, **123**, **125a**, **125b**, **125c**, **125d**, **125e**, and **125f** including the driving gate electrode (i.e., the first storage capacitor plate **125a**) are formed on the first insulating layer **141**.

A second insulating layer **142** is formed to cover the gate wires **121**, **122**, **123**, **125a**, **125b**, **125c**, **125d**, **125e**, and **125f** and the first insulating layer **141**. The first insulating layer **141** and the second insulating layer **142** are made of a silicon nitride (SiNx) or a silicon oxide (SiO_x).

The data wires **171a**, **171b**, **172a**, **172b**, and **178** including the upper data line **171a** and the lower data line **171b** spaced from each other, the upper driving voltage line **172a** including the second storage capacitor plate **178**, and the lower driving voltage line **172b** are formed on the second storage capacitor plate **178**.

The data wires **171**, **172a**, **172b**, and **178** may be formed of a triple layer of titanium/aluminum/titanium (Ti/Al/Ti), and as aluminum is a low-resistive metal, a voltage drop can be prevented.

As described, the second storage capacitor plate **178** is formed of the same or substantially the same material in the same layer of the second driving voltage line **172b** and the data line **171**, and therefore the second storage capacitor layer is not formed in an additional layer, thereby reducing the number of masks used in a manufacturing process. Thus, manufacturing cost can be reduced by reducing the number of masks in consideration of a cost per mask, and manufacturing time can be shortened.

In addition, the second storage capacitor plate **178**, the driving voltage line **172**, and the data line **171** are formed in the same layer and therefore no additional insulating layer for insulation of the second storage capacitor plate **178**, the driving voltage line **172**, and the data line **171** is needed, and a short-circuit between the second storage capacitor plate **178**, the driving voltage line **172**, and the data line **171** can be fundamentally prevented.

A passivation layer **180** is formed on the data wires **171**, **172a**, **172b**, and **178** and the second insulating layer **142** for protection thereof. The passivation layer **180** may be formed of an organic layer. The pixel electrode **191**, the first pixel connecting member **193**, the third pixel connecting member **194**, the second pixel connecting member **195**, and the initialization voltage line **192** are formed on the passivation layer **180**.

The plurality of contact holes **61**, **62**, **63**, **64**, **65**, **81**, **82**, **83**, **84**, and **85** are formed in the first insulating layer **141**, the second insulating layer **142**, and the passivation layer **180**, and the plurality of contact holes **61**, **62**, **63**, **64**, **65**, **81**, **82**, **83**, **84**, and **85** include first contact holes **62**, **63**, **64**, **65** formed only in the passivation layer **180**, second contact holes **81**, **82**, **83**, **84**, and **85** formed in the first insulating

layer **141**, the second insulating layer **142**, and the passivation layer **180**, and a third contact hole **61** formed in the second insulating layer **142** and the passivation layer **180**.

The pixel electrode **191** is connected with the light emission control drain electrode **177f** through the second contact holes **81** formed in the first insulating layer **141**, the second insulating layer **142**, and the passivation layer **180**, the initialization voltage line **192** is connected with the initialization source electrode **176d** through the second contact hole **82** formed in the first insulating layer **141**, the second insulating layer **142**, and the passivation layer **180**, a first end of the third pixel connecting member **194** is connected with the initialization drain electrode **177d** through the second contact hole **83** concurrently (e.g., simultaneously) formed in the first insulating layer **141**, the second insulating layer **142**, and the passivation layer **180**, and a second end of the third pixel connecting member **194** is connected with the driving gate electrode **125a** through the third contact hole **61** concurrently (e.g., simultaneously) formed in the second insulating layer **142** and the passivation layer **180**.

In addition, the upper data line **171a** and the lower data line **171b** are connected with the first pixel connecting member **193** through the first contact holes **62** and **63** formed in the passivation layer **180**, and the first pixel connecting member **193** is directly connected with the switching source electrode **176b** through the second contact hole **85** concurrently (e.g., simultaneously) formed in the first insulating layer **141**, the second insulating layer **142**, and the passivation layer **180**. The upper driving voltage line **172a** and the lower driving voltage line **172b** are respectively connected with the second pixel connecting member **195** through the first contact holes **64** and **65** formed in the passivation layer **180**, and the second pixel connecting member **195** is directly connected with the operation control source electrode **176e** through the second contact hole **85** concurrently (e.g., simultaneously) formed in the second insulating layer **142** and the passivation layer **180**.

A side wall **350** covering the passivation layer **180**, the first pixel connecting member **193**, the third pixel connecting member **194**, the second pixel connecting member **195**, the initialization voltage line **192**, and the pixel electrode **191** is formed at edges of the passivation layer **180**, the first pixel connecting member **193**, the third pixel connecting member **194**, the second pixel connecting member **195**, the initialization voltage line **192**, and the pixel electrode **191**, and the side wall **350** includes a side wall opening **351** exposing the pixel electrode **191**. The side wall **350** may be made of a resin such as a polyacrylate resin and a polyimide, or a silica-based inorganic material.

The organic emission layer **370** is formed on the pixel electrode **191** exposed by the side wall **351**, and the common electrode **270** is formed on the organic emission layer **370**. As described, the organic light emitting diode OLED including the pixel electrode **191**, the organic emission layer **370**, and the common electrode **270** is formed.

Here, the pixel electrode **191** becomes an anode, which is a hole injection electrode, and the common electrode **270** becomes a cathode, which is an electron injection electrode. However, an exemplary embodiment of the present disclosure is not limited thereto, and according to a driving method of the organic light emitting device, the pixel electrode **191** may be a cathode and the common electrode **270** may be an anode. The hole and electron are injected into the organic emission layer **370** from the pixel electrode **191** and the common electrode **270**, respectively, and an exciton gener-

ated by coupling the injected hole and electron falls from an excited state to a ground state to emit light.

The organic emission layer **370** is made of a low-molecular weight organic material or a high-molecular weight organic material such as poly(3,4-ethylenedioxythiophene) (PEDOT). Further, the organic emission layer **370** may be formed as a multilayer including an emission layer and one or more of a hole injection layer (HIL), a hole transporting layer (HTL), an electron transporting layer (ETL), and an electron injection layer (EIL). In the case where the organic emission layer **370** includes all the layers, the hole injection layer (HIL) is disposed on the pixel electrode **191** which is an anode, and the hole transporting layer (HTL), the emission layer, the electron transporting layer (ETL), the electron injection layer (EIL) are sequentially laminated thereon.

The organic emission layer **370** may include a red organic emission layer emitting red light, a green organic emission layer emitting green light, and a blue organic emission layer emitting blue light. The red organic emission layer, the green organic emission layer, and the blue organic emission layer are formed in a red pixel, a green pixel, and a blue pixel, respectively, thereby implementing a color image.

Further, the organic emission layer **370** may implement the color image by laminating the red organic emission layer, the green organic emission layer, and the blue organic emission layer together in the red pixel, the green pixel, and the blue pixel, and forming a red color filter, a green color filter, and a blue color filter for each pixel. As another example, white organic emission layers emitting white light are formed in all of the red pixel, the green pixel, and the blue pixel, and a red color filter, a green color filter, and a blue color filter are formed for each pixel, thereby implementing the color image. In the case of implementing the color image by using the white organic emission layer and the color filters, a deposition mask for depositing the red organic emission layer, the green organic emission layer, and the blue organic emission layer on respective pixels, that is, the red pixel, the green pixel, and the blue pixel, does not need to be used.

The white organic emission layer described in another example may be formed by one organic emission layer, and includes a configuration formed so as to emit white light by laminating a plurality of organic emission layers. For example, the white organic emission layer may include a configuration which may emit white light by combining at least one yellow organic emission layer and at least one blue light emitting layer, a configuration which may emit white light by combining at least one cyan organic emission layer and at least one red light emitting layer, a configuration which may emit white light by combining at least one magenta organic emission layer and at least one green light emitting layer, and the like.

An encapsulation member (not illustrated) protecting the organic light emitting diode OLED may be formed on the common electrode **270**, the encapsulation member may be encapsulated on the substrate **110** by a sealant, and may be made of various materials such as glass, quartz, ceramic, plastic, and metal. Meanwhile, a thin film encapsulation layer may be formed by depositing an inorganic layer and an organic layer on the common electrode **270** without using the sealant.

Hereinafter, a method for manufacturing an organic light emitting display device according to an exemplary embodiment of the present disclosure will be described with reference to the accompanying drawing.

FIG. 7, FIG. 10, and FIG. 13 are sequential layout views of a manufacturing method of an organic light emitting

display device according to an exemplary embodiment of the present disclosure, FIG. 8 is a cross-sectional view of the organic light emitting display device of FIG. 7, taken along the line VIII-VIII, FIG. 9 is a cross-sectional view of the organic light emitting display device of FIG. 7, taken along the line IX-IX, FIG. 11 is a cross-sectional view of the organic light emitting display device FIG. 10, taken along the line XI-XI, FIG. 12 is a cross-sectional view of the organic light emitting display device of FIG. 10, taken along the lines XII-XII' and XII'-XII'', FIG. 14 is a cross-sectional view of the organic light emitting display device of FIG. 13, taken along the line XIV-XIV, and FIG. 15 is a cross-sectional view of the organic light emitting display device of FIG. 13, taken along the lines XV-XV' and XV'-XV''.

First, as shown in FIG. 7 through FIG. 9, a buffer layer 120 is formed on a substrate 110. The buffer layer 120 may be formed as a single layer of a silicon nitride or a dual layer structure in which a silicon nitride and a silicon oxide are laminated, and is deposited to the entire surface on the substrate 110 using a plasma enhanced chemical vapor deposition (PECVD) method or the like. In addition, a semiconductor layer 130 is formed on the buffer layer 120. The semiconductor 130 may be formed of a polycrystalline semiconductor layer or an oxide semiconductor layer, and the polycrystalline semiconductor layer may be formed by forming an amorphous silicon layer and then crystallizing the amorphous silicon layer. Various suitable methods may be applied as a crystallization method, and the amorphous silicon layer may be crystallized using, for example, heat, laser, Joule heat, an electric field, or a catalyst metal. In addition, a photolithography process is performed using a first mask on the polycrystalline semiconductor layer such that the polycrystalline layer is patterned to a semiconductor 130 having a shape shown in FIG. 7. The semiconductor 130 has not been doped yet and thus is not divided into a channel, a source electrode, and a drain electrode forming each transistor.

Next, as shown in FIG. 10 through FIG. 12, a first insulating layer 141 covering the buffer layer 120 and the semiconductor 130 is formed on the buffer layer 120 and the semiconductor 130. The first insulating layer 141 is formed by wholly depositing a silicon nitride (SiNx) or a silicon oxide (SiO_x) using a PECVD method or the like. In addition, a gate metal layer is deposited to the first insulating layer 141. Further, the gate metal layer is patterned through a photolithography process using a second mask. Thus, gate wires including a scan line 121, a previous scan line 122, a light emission control line 123, a bypass control line 128, and a driving gate electrode 125a are formed. The gate metal layer may be made of a multi-layer of a metal layer including at least one of copper (Cu), a copper alloy, aluminum (Al), and an aluminum alloy and a metal layer including at least one of molybdenum (Mo) and a molybdenum alloy.

In addition, an impurity is doped to the semiconductor 130. The semiconductor 130 is doped with the impurity, excluding portions respectively covered by a switching gate electrode 125b, a compensation gate electrode 125c, an initialization gate electrode 125d, an operation control gate electrode 125e, a light emission gate electrode 125f, a bypass gate electrode 125g, and a driving gate electrode 125a. Thus, a source electrode and a drain electrode of each transistor are formed. A channel of each transistor is formed in the semiconductor 130 in areas which are not doped. That is, a driving channel 131a, a switching channel 131b, a compensation channel 131c, an initialization channel 131d, an operation control channel 131e, a light emission control

channel 131f, and a bypass channel 131g are concurrently (e.g., simultaneously) formed. As described, no additional mask is required in doping of the semiconductor 130.

Next, as shown in FIG. 13 through FIG. 15, a second insulating layer 142 covering the first insulating layer 141, the scan line 121, the previous scan line 122, the light emission control line 123, the bypass control line 128, and the driving gate electrode 125a is formed on the first insulating layer 141, the scan line 121, the previous scan line 122, the light emission control line 123, the bypass control line 128, and the driving gate electrode 125a. The first insulating layer 141 is formed by wholly depositing a silicon nitride (SiNx) or a silicon oxide (SiO_x) using a PECVD method or the like. In addition, a dopant activation process is performed to make the impurity doped in the semiconductor 130 settled therein, and damage to an interface between the semiconductor 130 and the first insulating layer 141 is prevented.

A data metal layer is formed on the second insulating layer 142. The data metal layer may be formed of a multi-layer of a metal layer including at least one of copper, a copper alloy, aluminum, and an aluminum alloy and a metal layer including at least one of molybdenum and a molybdenum alloy. For example, the data metal layer may be formed of a triple layer of titanium/aluminum/titanium (Ti/Al/Ti) or a triple layer of molybdenum/copper/molybdenum (Mo/Cu/Mo).

The data metal layer is patterned through a photolithography process using a third mask. Thus, the data wires including the upper data line 171a and the lower data line 171b spaced from each other by the distance d1 and the upper driving voltage line 172a and the lower driving voltage line 172b spaced from each other by the distance d2 is formed on the interlayer insulating layer 160. The second storage capacitor plate 178 is a part expanded (e.g., protruded or extended) from the upper driving voltage line 172a. As described, the second storage capacitor plate 178 is formed of the same or substantially the same material and in the same layer as the driving voltage line 172 and the data line 171 so that there is no need for forming the second storage capacitor plate in an additional layer, and accordingly the number of masks used in the manufacturing process can be reduced.

Next, as shown in FIG. 4 through FIG. 6, a passivation layer 180 covering the data lines 171a, 171b, 172a, 172b, and 178 is formed on the second insulating layer 142, and the plurality of contact holes 61, 62, 63, 64, 65, 81, 82, 83, 84, and 85 are formed in the passivation layer 180 through a photolithography process using a fourth mask. In addition, a dry etching process is additionally performed to additionally etch the first insulating layer 141 and the second insulating layer 142 exposed in the contact holes 81, 82, 83, 84, and 85 to thereby expose the semiconductor 130 therebelow, and at the same time, the second insulating layer 142 exposed in the contact hole 61 is additionally etched to expose the driving gate electrode 125a therebelow. Thus, the first contact holes 62, 63, 64, and 64 formed only in the passivation layer 180, the second contact holes 81, 82, 83, 84, and 85 formed together in the second insulating layer 142 and the passivation layer 180, and the third contact hole 61 formed in the second insulating layer 142 and the passivation layer 180 are formed. As described, in a conventional exemplary embodiment of the present disclosure in which the contact hole is formed in the inorganic insulating layer using an additional mask, a dry etching process is additionally performed in the contact hole formed in the passivation layer 180 and thus the contact hole can be

formed in the inorganic insulating layer without using an additional mask, thereby reducing the number of masks.

In addition, a pixel electrode layer is formed on the passivation layer **180** and the pixel electrode layer is patterned through a photolithography process using a fifth mask. Thus, the pixel electrode **191** which is directly connected with the light emission control drain electrode **177f** through the contact hole **81**, the initialization voltage line **192** which is connected with the initialization source electrode **176d** through the contact hole **82**, the first pixel connecting member **193** which is connected with the upper data line **171a**, the lower data line **171b**, and the switching source electrode **176d** through the contact holes **62**, **63**, and **84**, the third pixel connecting member **194** which is connected with the initialization drain electrode **177d** and the driving gate electrode **125a** through the contact holes **83** and **61**, and the second pixel connecting member **195** which is connected with the upper driving voltage line **172a**, the lower driving voltage line **172b**, and the operation control source electrode **176e** through the contact holes **62**, **63**, and **84** are formed.

In addition, a side wall **350** covering the pixel electrode **191**, the initialization voltage line **192**, the first pixel connecting member **193**, the third pixel connecting member **194**, and the second pixel connecting member **195** is formed on the passivation layer **180**, and a side wall opening **351** that partially exposes the pixel electrode **191** is formed in the side wall **350** using a sixth mask. An organic emission layer **370** is formed on the pixel electrode **191** exposed through the side wall opening **351** of the side wall **350**. In addition, a common electrode **270** is formed on the organic emission layer **370** such that an organic light emitting element **70** is formed. The common electrode **270** is formed throughout the entire area, excluding above the side wall **350**, so that no additional mask is used.

While this disclosure has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the present disclosure is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims and their equivalents.

Description of some of the symbols

121: scan line	122: previous scan line
123: light emission control line	124: initialization voltage line
125a: driving gate electrode	125b: switching gate electrode
131a: driving channel	131b: switching channel
141: first gate insulating layer	142: second gate insulating layer
171: data line	171a: upper data line
171b: lower data line	172: driving voltage line
172a: upper driving voltage line	172b: lower driving voltage line
180: passivation layer	191: pixel electrode
192: initialization voltage line	193: first pixel connecting member
195: second pixel connecting member	
194: third pixel connecting member	
270: common electrode	370: organic emission layer

What is claimed is:

1. An organic light emitting display device comprising:
 - a substrate;
 - a semiconductor on the substrate and comprising:
 - a switching channel of a switching transistor; and
 - a driving channel of a driving transistor, the driving transistor being spaced from the switching transistor;
 - a first insulating layer covering the semiconductor;

a switching gate electrode on the first insulating layer and overlapping the switching channel;

a driving gate electrode on the first insulating layer and overlapping the driving channel;

a second insulating layer covering the switching gate electrode and the driving gate electrode;

a data line on the second insulating layer and configured to transmit a data signal comprising:

an upper data line; and

a lower data line spaced from the upper data line;

a driving voltage line on the second insulating layer and configured to transmit a driving voltage;

a passivation layer covering the data line and the driving voltage line;

a pixel electrode on the passivation layer; and

a first pixel connecting member on the passivation layer and connecting the upper data line and the lower data line.

2. The organic light emitting display device of claim 1, wherein the first pixel connecting member is connected with the upper data line and the lower data line through one or more first contact holes in the passivation layer.

3. The organic light emitting display device of claim 2, wherein the semiconductor comprises:

a switching source electrode at a side of the switching channel; and

a switching drain electrode at another side of the switching channel, and

wherein the first pixel connecting member is connected with the switching source electrode through a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

4. The organic light emitting display device of claim 1, further comprising:

a second pixel connecting member on the passivation layer,

wherein the driving voltage line comprises:

an upper driving voltage line; and

a lower driving voltage line spaced from the upper driving voltage line, and

wherein the second pixel connecting member connects the upper driving voltage line and the lower driving voltage line.

5. The organic light emitting display device of claim 4, wherein the second pixel connecting member is connected with the upper driving voltage line and the lower driving voltage line through a first contact hole in the passivation layer.

6. The organic light emitting display device of claim 5, further comprising:

a scan line connected with the switching gate electrode and configured to transmit a scan signal;

a light emission control line in a same layer as the scan line and configured to transmit a light emission control signal; and

an operation control transistor comprising:

an operation control gate electrode, which is a part of the light emission control line;

an operation control source electrode in the semiconductor; and

an operation control drain electrode in the semiconductor,

wherein the second pixel connecting member is connected with the operation control source electrode through a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

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7. The organic light emitting display device of claim 6, further comprising:

a compensation transistor comprising:

a compensation gate electrode, which is a part of the scan line;

a compensation source electrode in the semiconductor; and

a compensation drain electrode in the semiconductor; and

a third pixel connecting member in the same layer as the pixel electrode and connecting the driving gate electrode and the compensation drain electrode.

8. The organic light emitting display device of claim 7, wherein the third pixel connecting member is connected with the compensation drain electrode through another second contact hole and is connected with the driving gate electrode through a third contact in the second insulating layer and the passivation layer.

9. The organic light emitting display device of claim 6, further comprising:

a previous scan line in the same layer as the scan line and configured to transmit a previous scan signal;

an initialization voltage line in the same layer as the pixel electrode and configured to transmit an initialization voltage line; and

an initialization transistor comprising:

an initialization gate electrode, which is a part of the previous scan line;

an initialization source electrode in the semiconductor; and

an initialization drain electrode in the semiconductor, wherein the initialization voltage line is connected with the initialization source electrode through another second contact hole.

10. The organic light emitting display device of claim 6, further comprising:

a light emission control transistor comprising:

a light emission control gate electrode, which is a part of the light emission control line;

a light emission control source electrode in the semiconductor; and

a light emission control drain electrode in the semiconductor,

wherein the pixel electrode is connected with the light emission control drain electrode through another second contact hole.

11. The organic light emitting display device of claim 1, further comprising:

a storage capacitor overlapping the driving gate electrode, wherein the storage capacitor comprises:

a first storage capacitor plate, which is the driving gate electrode; and

a second storage capacitor plate overlapping the first storage capacitor plate and on the second insulating layer, and

wherein the second storage capacitor plate is an expanded area of an upper driving voltage line.

12. The organic light emitting display device of claim 11, wherein the driving channel comprises at least one curved portion.

13. The organic light emitting display device of claim 1, further comprising:

an organic emission layer on the pixel electrode; and a common electrode covering the organic emission layer.

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14. A method for manufacturing an organic light emitting display device, comprising:

forming a semiconductor on a substrate;

forming a first insulating layer on the semiconductor;

forming a driving gate electrode of a driving transistor and a switching gate electrode of a switching transistor on the first insulating layer;

forming a driving channel and a switching channel in the semiconductor provided under the driving gate electrode and the switching gate electrode by performing a doping process;

forming a second insulating layer covering the driving gate electrode and the switching gate electrode;

forming a data line comprising an upper data line and a lower data line that are spaced from each other on the second insulating layer;

forming a passivation layer covering the data line; and forming a pixel electrode and a first pixel connecting member on the passivation layer,

wherein the first pixel connecting member connects the upper data line and the lower data line.

15. The method for manufacturing the organic light emitting display device of claim 14, further comprising:

forming a contact hole in the passivation layer after forming the passivation layer; and

exposing the semiconductor by etching the first insulating layer and the second insulating layer exposed in the contact hole by performing a dry etching process in the contact hole,

wherein the contact hole comprises a first contact hole only in the passivation layer and a second contact hole in the first insulating layer, the second insulating layer, and the passivation layer.

16. The method for manufacturing the organic light emitting display device of claim 15,

wherein the first pixel connecting member is connected with the upper data line and the lower data line through the first contact hole and connected with the semiconductor through the second contact hole.

17. The method for manufacturing the organic light emitting display device of claim 15,

wherein the forming the data line comprises:

forming a driving voltage line comprising:

an upper driving voltage line; and

a lower driving voltage line spaced from the upper driving voltage line, and

wherein forming the first pixel connecting member comprises:

forming a second pixel connecting member that connects the upper driving voltage line and the lower driving voltage line.

18. The method for manufacturing the organic light emitting display device of claim 17,

wherein the second pixel connecting member is connected with the upper driving voltage line and the lower driving voltage line, through the first contact hole, and is connected with the semiconductor through the second contact hole.

19. The method for manufacturing the organic light emitting display device of claim 14,

wherein, after forming the second insulating layer, a dopant activation process is performed at the semiconductor to eliminate damage to an interface between the semiconductor and the insulating layer.

* * * * *

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摘要(译)

根据本公开的有机发光显示装置包括：基板上的半导体，其包括开关晶体管的开关沟道和驱动晶体管的驱动沟道，所述驱动晶体管与所述开关晶体管间隔开；覆盖所述半导体的第一绝缘层；在所述第一绝缘层上并且与所述开关沟道重叠的开关栅电极，以及在所述第一栅绝缘层上并与所述驱动沟道重叠的驱动栅电极；覆盖所述开关栅电极和所述驱动栅电极的第二绝缘层；在所述第二绝缘层上的数据线包括：上数据线和下部数据线；在所述第二绝缘层上的驱动电压线；钝化层，覆盖所述数据线和所述驱动电压线；在所述钝化层上的像素电极；以及在所述钝化层上的第一像素连接构件。

